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TI REPORT NUMBER
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THIRD QUARTERLY PROGRESS REPORT
FOR
MATERIAL PROCESSING AND PHENOMENA INVESTIGATION
OF
FUNCTIONAL ELECTRONIC BLOCKS

CONTRACT AF 33(657)-9196

TEXAS INSTRUMENTS INCORPORATED

13500 NORTH CENTRAL EXPRESSWAY • DALLAS, TEXAS

This Report Covers the Period 1 March 1963 through 31 May 1963

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Texas Instruments Incorporated
13500 North Central Expressway
Dallas 22, Texas

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SUMMARY

Work has proceeded as follows:

Task I

1. GaAs epitaxial deposition technology has been optimized to include effects of seed orientation, vapor stream composition, temperature, and thermal gradient.

2. Diffusion of zinc from doped SiO_2 is well characterized and is used routinely.

3. Work on diffusion of Te and a double diffused transistor structure has been started.

Task II

1. GaAs epitaxial deposition in a closed system is routine, but we have not deposited high resistivity GaAs.

2. Voltage breakdown mechanisms and parameters have been studied for various high resistivity samples.

Task III

1. Doped CdS preparation is routine and material is being supplied for work on Contract No. AF 33(657)-9824.

2. Indium diffusion for surface treatment of high resistivity CdS is routine.

3. Contact studies are still under way, with only minor advances during the third quarter.

4. A comprehensive analysis of the photocapacitor is presented.

Task IV

1. $GaAs_xP_{(1-x)}$ has been prepared for all values of x.
2. Adherent layers of GaP have been produced on a GaAs seed by use of an intermediate layer of $GaAs_xP_{(1-x)}$.

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I. WORK STATEMENT OF THE CONTRACT

Research efforts are as follows:

1. Use of high resistivity GaAs as a substrate for functional electronic blocks.
2. Investigation of problems associated with three dimensional arrays.
3. Investigation of phenomena (particularly photon-induced actions) in II-VI compounds as amenable to further functional electronic block designs.
4. Investigation of GaP and GaAsP epitaxial growth with various doping agents for electroluminescent devices.

II. DESCRIPTION OF TASKS

A. Task I--High Resistivity GaAs Substrates

During this quarter we have concentrated on:

1. Epitaxial deposition of GaAs on GaAs
2. Masking and diffusion techniques applicable to FEB's
3. Planning of the transistor structure to be used in the FEB.

The proposed objectives for Task I are more than 70 percent complete. No difficulty is expected to prevent successful completion of the task except for the deposition of epitaxial silicon on GaAs.

GaAs Epitaxial Layers on GaAs

The long range goal of this subtask is to provide the GaAs epitaxial material necessary for device development on this contract. A number of problem areas have been identified and are listed below.

1. The epitaxial layer should have a good surface when the deposition is completed. Use of the material by the device groups will involve further diffusions and alloyings, and a smooth surface will lead to the best junction formation after these techniques are used. Visual observation or a cursory microscopic examination is generally sufficient to show the presence of gross surface structure. In our deposition process we have found that a good surface on the substrate is necessary but is not sufficient to produce a good surface on the deposit. The closer the crystal orientation is to a (111) direction, the better the texture of the final surface. However, as a perfect orientation is approached, the deposition rate seems to decrease.

2. A reasonably rapid deposition rate is also necessary. As the device work develops and large numbers of diffusions must be run and evaluations made on large numbers of slices, the problem of supplying material becomes more and more acute. Layers of material from 10 to 25 microns are required for device work, and as noted above, the surface structure improves as the deposition rate decreases. It may be necessary, therefore, to

sacrifice a faster deposition rate for better surface preparation. If the surface is irregular, part of it must be lapped off to achieve the flat surface necessary for device work. Deposits 2 to 3 times as thick (20 to 30 microns thick compared to 10 microns) may be required to retain a reasonable amount of the epitaxial deposit after lapping.

3. A high purity deposit, both chemically pure and physically as perfect as possible, is desirable. We hope that our method will produce much purer GaAs than does crystal pulling or ingot growing and that we will be able to take advantage of the intrinsic properties of the GaAs.

4. An electrical evaluation or an evaluation in terms of the device possibilities of the material is necessary. Since we are dealing with a special form of GaAs, a very thin layer which may or may not be on an insulating substrate, new electrical evaluation techniques are necessary. In general, the methods previously developed for measuring Hall effect and resistivity and for deriving the mobility of GaAs are not directly applicable to the epitaxial layers we are working with.

5. We are striving to develop techniques to prepare a wide range of dopings of GaAs so that we will be able to produce material on demand as specified by the device development groups. This would include control of n- and p-type dopants to desired impurity concentrations as well as high purity GaAs as noted above. We would like also to be able to control the number of physical defects such as vacancies and dislocations.

With these problem areas and subtasks in mind, we can discuss the work which has been done during the third quarter to achieve the material required.

In our original deposition work reported previously, we used GaAs as the feed material for the vapor stream from which deposition occurs. In much of the work since then we have continued to use GaAs as the feed material, largely because the material is available and it is necessary only to pass a stream of hydrogen plus $AsCl_3$ over the feed to get the proper vapor

composition. There are a number of disadvantages in using GaAs as the feed material, mainly the dependence upon another preparation step which determines the purity of the feed. Bulk GaAs prepared by standard methods can become accidentally contaminated by chemical impurities. These chemical impurities will be carried over into the epitaxial material when the contaminated GaAs is used as the feed material. This difficulty is obviated by using elemental Ga as a source in GaAs deposition, though the process is much more difficult. We successfully used this process during the last quarter, and the preliminary results are reported here.

The chemical reactions which we believe occur during the depositions are as follows:

$$\text{GaAs (or Ga)} + H_2 + AsCl_3 \rightarrow Ga_xCl_y + H_2 + As_4 + HCl + AsCl_3 \qquad (1)$$

$$Ga_xCl_y + H_2 + As_4 + HCl + AsCl_3 \rightarrow \text{GaAs + excess reactants} \qquad (2)$$

The first equation represents the vaporization of feed material, either GaAs or Ga, when excess H_2 and $AsCl_3$ are passed over it. The temperature is approximately 900°C in our process. The products in Eq. (1) are all gaseous at that temperature. The second equation represents the deposition of GaAs at a lower temperature, 750°C, for instance. All excess reactants in the reaction are gaseous at this temperature and are carried downstream by the gas flow. If conditions are chosen properly, the GaAs will form a uniform epitaxial deposit on the seed. Because the composition of the gas stream carrying the material to the seed is very complex, it is impossible to describe exactly the chemical reactions occurring during deposition. It is much easier to study the deposition process empirically, that is, to vary one parameter such as the flow rate, the gas composition, the temperature of the source (whether Ga or GaAs), or the relative amounts of hydrogen or $AsCl_3$.

The effect of the variation has been studied in terms of the deposition rate, the surface appearance of the material, the electrical evaluation if possible, or the device performance. Such indirect methods of studying the deposition mean, of course, that more runs than usual must be made to establish the base line of deposition for comparison with the variable runs. In the discussion which follows we show the variation in deposition which results from the various parameters studied.

We have noted two major interactions of deposition on GaAs as a function of the orientation of the substrate: rate of growth and surface character, as revealed by visual observation. Table I summarizes the data from the various runs.

One conclusion which can be drawn from the data in Table I is that there seems to be no difference between the deposition on the B face ($\bar{1}\bar{1}\bar{1}$) and the deposition on the A face (111). This result agrees with some recent work reported by N. Goldsmith,[1] who found that the presence of considerable amounts of an acid species (HCl, in particular) decreases any growth difference.

Deposition in the (111) direction depends very much on the precision of the seed crystal orientation. Comparing the runs at ±7° off orientation with those ±1/2° off, we see that the latter gives a much better surface structure. The examination is made by microscope and is subject to personal interpretation. Figure 1 illustrates the phenomenon. Photographs of the epitaxial layer surface were taken at the magnification indicated. Photos (a) and (b) were of layers deposited on seeds about 1/2° off the (111) orientation; (c) and (d) were layers on seeds > 3° off. In the photos, the top faces of the pyramidal formations show the true (111) surfaces. The amount these pyramids project from the surface is a function of the misorientation of the substrate.

For otherwise equivalent conditions, the more closely oriented seeds

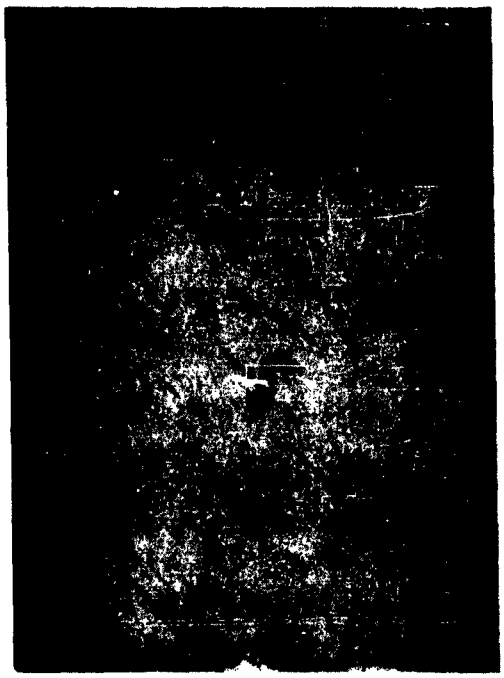
[1] N. Goldsmith, J. Electrochem. Soc. 110, 588(1963).

TABLE I

Effect of Orientation on GaAs Deposition*

Run	Substrate Orientation	$AsCl_3:H_2$ Ratio	Dep. Rate μ/hour	Remarks
751-28	(100)	1:14	7.5	Irregular, etched
-29	$(\bar{1}\bar{1}\bar{1})$ ±7°, B face	1:14	5.0	Triangular figuring on surface
-30	(111) ±7°, A	1:14	5.0	Triangular figuring on surface
-31	(111) ±7°, A	1:14	2.5	Triangular figuring on surface, plus irregularities along scratches
-33	$(\bar{1}\bar{1}\bar{1})$ ±1/2°, B	1:14	1.3	Very good surface
-34	$(\bar{1}\bar{1}\bar{1})$ ±1/2°, B	3:14	1.3	Very good surface
-35a	$(\bar{1}\bar{1}\bar{1})$ ±1/2°, B	3:14	3.0	Very good surface
-35b	$(\bar{1}\bar{1}\bar{1})$ ±7°, B	3:14	6.0	Same as 29 and 30

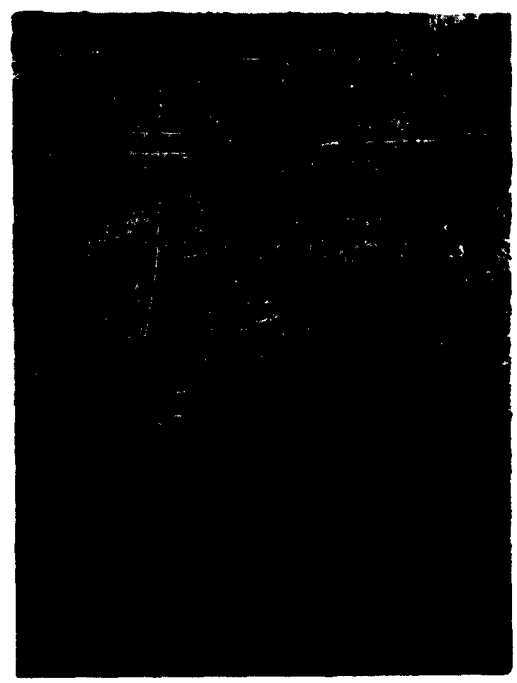
*All seeds were chemically polished except #31 which was mechanically polished. Seed temperature was 800°C, source temperature was 900°C except #35 where it was 950°C. The $AsCl_3:H_2$ represents ratio of H_2 flow through the $AsCl_3$ bubbler to the H_2 flow as make-up and dilution.



(a)

(b)

(c)



(d)

Fig. 1 Effect of seed orientation on surface structure of epitaxial deposit. All enlargements are 275X except (c) which is 387X. (a) and (b) are 1/2° off (111), (c) and (d) are > 3° off (111).

show a considerably lower rate of deposition. Deposition on the (100) oriented seed seems to be much faster than on the (111) orientation, but the deposit appearance is much poorer. For further work in device technology, we prefer the (111) orientation because of the isotropy of the layer with respect to alloying operations. Therefore, we have not seriously considered any depositions on orientations other than (111).

Some initial experiments were attempted using Ga rather than GaAs as a feed material. In these initial experiments we simply replaced the GaAs with Ga, using the apparatus as described in the second quarterly report. The deposition was not satisfactory. Deposits were produced, but they were very thin (about 1 micron) and were nonuniform. Most of the difficulties were caused by poor control of the gas stream, which reacted with the Ga. Presumably, not enough Ga could be picked up and carried to the deposition zone. Purity could not be evaluated because the deposits were so thin.

A new deposition reactor was constructed, taking into account the difficulties we found with the original reactor. Figure 2 is a diagram of the apparatus. It includes separately regulated supplies of As and Ga. Arsenic concentration in the gas phase is regulated by controlling the temperature of an As feed and by the proportion of hydrogen gas that passes over the As feed compared to the total hydrogen make-up. Ga is picked up from its source by passing HCl over the Ga boat. The problem of finding a source of HCl pure enough to be used in these experiments was solved by hydrogen reduction of $AsCl_3$ at 1000°. Ultra high purity $AsCl_3$ is prepared by distillation to use as a source of As for other reactions in our Laboratory. It contains very small amounts of chemical impurities. Hydrogen, purified by diffusion through palladium, is used to reduce the $AsCl_3$. The resulting gas stream contains a number of extraneous products which can be trapped out; the excess hydrogen and HCl then pass to the Ga feed system.

The versatility of the new reactor deposition system will permit a controlled study of stoichiometry in the deposits. In addition, it allows

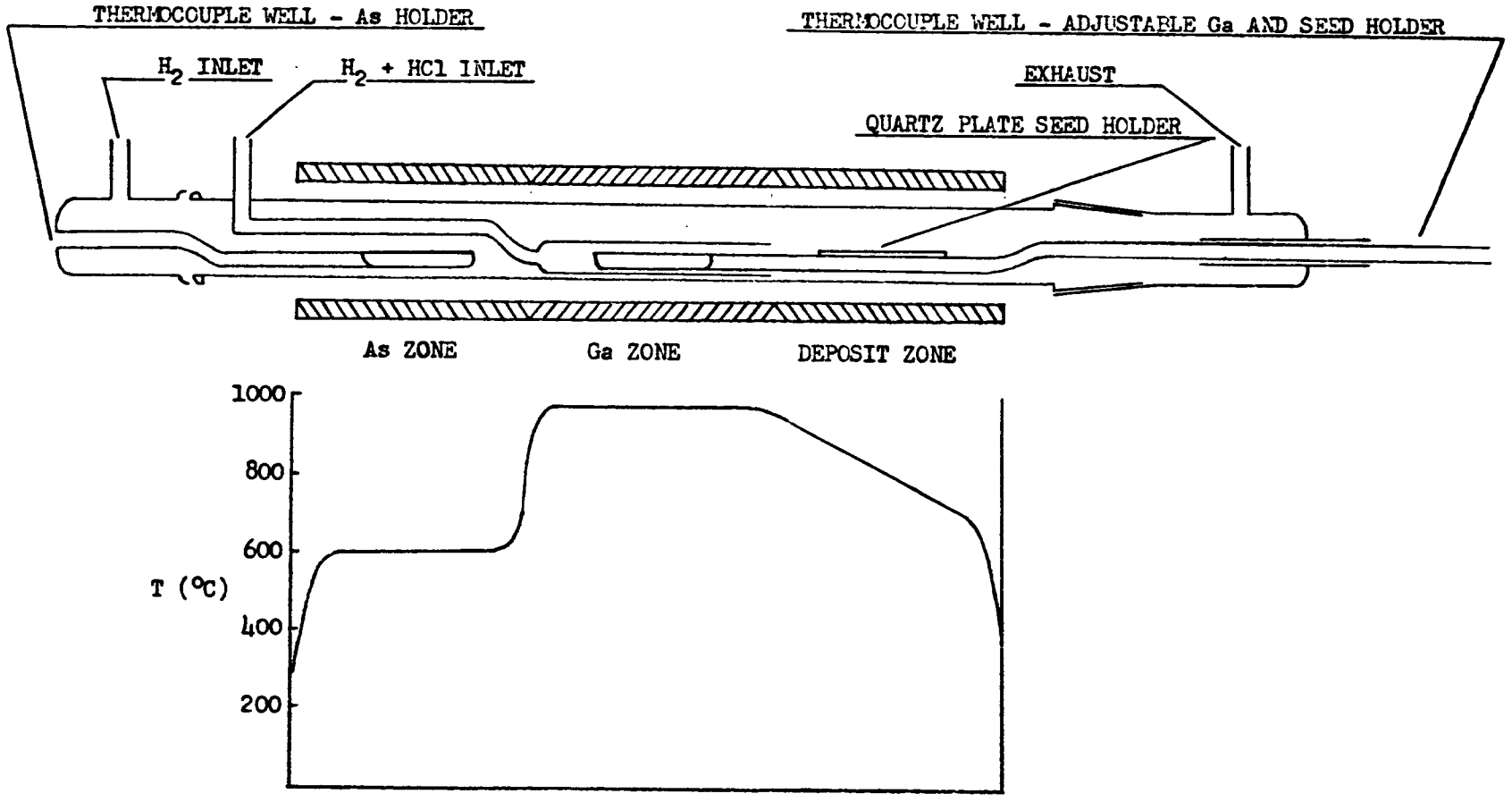


Fig. 2 System and temperature profile for the epitaxial deposition of GaAs employing elemental gallium and arsenic.

a purer deposition of GaAs because the conditions in handling the elemental materials and the gases can be better controlled. During the third quarter this new system was completed, but only a polycrystalline deposit was produced in the single run made. We will continue work on this system during the next quarter and will report the results.

A considerable number of experiments have been run with modified heat flow distributions in the GaAs seed to determine deposition rate dependence and physical condition of the deposit. In general, the seed on which deposition was to occur was set on a flat spot in the reactor, ensuring the best thermal contact possible with the reactor wall. The outside of the reactor at that point could be controllably cooled using a cooling block or an air stream impinging onto the reactor wall. We hoped this would produce a thermal gradient through the substrate and perpendicular to its surface. Under these conditions the gas stream inside the reactor would see a lowering temperature in the direction perpendicular to the seed surface. We might expect that a more rapid deposition rate will occur, though we must guard against a rate so rapid that the gas stream might become supersaturated, and many nucleation points might produce a polycrystalline deposit on the seed. Table II shows the results of the number of runs on this particular set of experiments. Runs 751-51 through 751-61 are concerned primarily with the effect of the thermal gradient on the deposition rate of the material. In general, a steeper thermal gradient leads to a faster deposition rate. The remaining runs described in the table are attempts to determine the effect of the $AsCl_3$ concentration on the deposition rate and the temperature at which deposition takes place.

We plan to continue studies on the deposition rate and surface structure in the coming months; however, on the basis of the last quarter's work we can draw the following conclusions:

1. Deposition on the (100) face is faster than on the (111), but the deposit is more irregular.

TABLE II

Epitaxial Deposition in GaAs-Flow System

Run No.	H_2:$AsCl_3$ Ratio	Deposit Time (hrs)	Thickness	Remarks
751-51		2	7μ	Deposits fair. Used for
-52		2	15μ	device studies.
-53		4	20μ	Surface irregular due to A-face chem-polish.
-56		3	6μ	Gas cooled block to give
-57		3	22μ	proper heat flow. Good deposits visually.
-58		3	21.7μ	Thermal gradient steep.
-59		3	0 to 17.5μ	Thickness increased as thermal gradient increased.
-60		5	23.3μ	Steep thermal gradient.
-61		5	52.2μ	Steep thermal gradient.
778-9	15	5	41μ 34μ 30μ	Three seeds at decreasing temperature as thickness decreased.
-10	35	4	88μ 83μ	Two seeds. 88μ deposit at higher temperature.
-12	25	5	12μ	Polycrystalline. Poor
-13	25	5	66μ	thermal gradient.

All seeds chem-polished prior to deposition. B-face ($\bar{1}\bar{1}\bar{1}$) deposition except A-face in 751-53. Deposition temperature 800°C in 751-57, 800° ± 25°C in 778-9, -10, -12, -13, GaAs source at 950°C. Constant flow rate of hydrogen and $AsCl_3$ in all experiments except as noted.

2. The closer the seed orientation is to the (111), the slower the deposition, but the better the surface appearance of the deposit.

3. A higher $AsCl_3$ ratio in the gas stream leads to a faster deposition rate up to a certain point.

4. Higher seed temperatures, 825° to 830°C, compared to 800°C, lead to faster deposition rates.

5. A steeper thermal gradient perpendicular to the seed surface leads to a faster deposition rate.

To complete the range of technologies available to us we are building a deposition system to produce doped deposits. The apparatus will not differ greatly from those now in use for undoped depositions. We plan to introduce the impurities as volatile compounds, gaseous at the temperature of the system. The major change from our present systems will be the addition of metering systems and plumbing needed to introduce the dopes. Because of the presence of these impurities and the possibility of accidental doping, we will not use the new system to produce undoped material. Nor can we temporarily use one of our present deposition systems and hope to achieve the purity now possible after the system is returned to producing undoped material. For introducing donor impurities we expect to use H_2S or H_2Se, and for acceptor impurities $ZnCl_2$ or $CdCl_2$ will be used. After we have shown the possibility of acceptor doping we hope to be able to deposit high resistivity GaAs by special doping treatment during deposition.

Electrical evaluation of all our epitaxial GaAs layers remains a difficult problem to overcome. For bulk GaAs the electrical measurements and their interpretations are exceedingly complex, much more so than for bulk elemental semiconductors. Extending the measurements to epitaxial semiconductor compounds increases the difficulties still further, and the interpretations of measurements are still subject to doubt at present. We have been able to make some measurements on epitaxial GaAs deposited on high resistivity substrates, though the exact contribution of the intermediate layer between the deposited layer and the high resistivity substrate is in question. Furthermore, the problems of making contacts have not been completely solved. We have not been

able to extend our measurements to epitaxial GaAs layers deposited on low resistivity substrates. Allowing for these difficulties, we can report on some preliminary evaluations of epitaxial layers, subject to further corrections as our interpretation improves. The deposits reported in Table III were on high resistivity substrates, and contact was made to the epitaxial layer by using silver paint. It was assumed that the substrate made no contribution to electrical effects. Since the techniques we are using are changing, we will not report on them in detail here. A technical note will be submitted for review in the coming month and will give much more detail concerning these measurements.

The data in Table III are conflicting, but they indicate a material whose quality is not high compared to bulk GaAs. In particular, the mobility is not good, usually indicating either large numbers of charged impurities or physical defects acting as scattering centers. As a cross-check, we have made alloyed diodes from some of our deposits, and these diodes indicate a much better material than does the electrical evaluation. Diodes were made from deposits 751-20, oriented (100). Ohmic contact was made by alloying a tab (1% Se in Au, plated onto platinum) to the substrate. Rectifying contact was made by alloying a wire (4% Zn in Au) into the deposit. The diodes gave PIV's of 225 volts, 250 volts, 280 volts, and more than 300 volts. (Similar diodes made in the substrate gave PIV's of about 20 volts.) As reported below in the section on diffusion work, some of these deposits have been made into diffused diodes and similar results are seen. This conflict between the electrical evaluation by usual means and the evaluation in devices is another indication of the lack of understanding of electrical evaluation.

Masking and Diffusion for Multiple Device Formation

Our operations in this subtask have been oriented primarily toward production of an operating functional electronic block in a GaAs epitaxial layer. In the past we have developed resistors and capacitors, and more recently, we have developed diodes and transistors by diffused techniques as described in this report. Much of the work has been carried on using bulk

TABLE III

Electrical Evaluation of GaAs Epitaxial Layers

Sample	Resistivity (Ω cm)		Mobility, cm^2/V sec		Carriers, cm^{-3}	
	300°K	77°K	300°K	77°K	300°K	77°K
751-19a	0.14	0.20	2200	1600	2×10^{16}	2×10^{16}
-21	0.039	0.040	1700	2000	9×10^{16}	8×10^{16}
-26	0.014	0.0087	450	950	1×10^{18}	8×10^{17}

Layers deposited on high resistivity substrate. Contact made by silver paint to deposited layer. We assume that the substrate makes no contribution to the measured values.

GaAs, partly for economic reasons and partly because epitaxial deposits are not readily available. Because of our success in producing better epitaxial materials this quarter, more work has been done on epitaxial material. We expect to increase the work on epitaxial material until we have achieved the contract goals.

It has become apparent that most of the problems associated with device formation have been caused by the lack of a good diffusion technology. Our work has emphasized this particular aspect of GaAs technology, almost to the exclusion of any other in this subtask during the third quarter. Essentially, we are trying to determine the conditions necessary to use diffusions routinely to prepare the device structure we require. We are rapidly approaching such a state of operation.

We have continued our study of diffusion of dopants from sputtered SiO_2 films reported in the second quarterly report. This subtask is divided into the following areas of work:

1. A study of the cleanliness of the sputtering system and its effect on the diffused layer. We are concerned here with both an accidental transfer of dope from doped sputtered film operation to undoped sputtered film operation, and also the accidental introduction of extraneous impurities by metallic parts of the sputtering system.
2. A study of the diffusion time, particularly of Zn, vs the depth of the junction produced.
3. A study of the junction capacitance, particularly as it relates to an evaluation of the type of junction produced in this method of diffusion.
4. Methods of producing planar diodes and transistor structures by using these diffusion techniques.
5. Some preliminary studies on the diffusion of n-type dopants through and from SiO_2 films.

6. The diffusion of zinc into epitaxial GaAs layers as a means of evaluating those layers in device formation.

The following operating conditions were used in all sputtering of SiO_2 onto GaAs described below:

Sputtering voltage	1800 volts
Current	60 ma
Oxygen pressure	40 microns
Deposition rate	1500 Å per hour

The sputtered layers are 7500 Å thick unless otherwise indicated. If a dopant is to be diffused from the sputtered layer into the GaAs, it is incorporated into the layer during the sputtering process. This process and the diffusions were reported at the Electrochemical Society Meeting in Pittsburgh, April, 1963, and a more comprehensive description of this work is being prepared for submission as a technical note to Aeronautical Systems Division. Further details will be available at that time.

After some completely unexplainable results in attempting to cover GaAs with undoped SiO_2 films, it became evident that undoped and doped films cannot be deposited in the same sputtering system without drastic cleaning procedures between runs. Thus, if zinc is used to co-deposit with a SiO_2 film, the entire sputtering apparatus must be acid-etched or replaced to avoid the appearance of zinc in later runs which may be otherwise undoped. Control runs demonstrated this conclusively. It is very inconvenient to change and clean the apparatus as thoroughly as required under these conditions, so separate sputtering rigs are used for doped and undoped depositions. We also found that extraneous metal contaminations (in particular, Fe, Mg, and Cu) appeared occasionally during the diffusion in some of our runs. These contaminations were traced to the mechanical drive mechanism used for the sample holder in the sputtering rig. Therefore, we redesigned and rebuilt all our sputtering rigs so that the internal parts are made only of aluminum, quartz, or Teflon. Spectrographic analysis of the sputtered films shows no impurities to the limit of our detectability. We have now achieved a satisfactory control of the purity of our sputtered layers.

We reported more thoroughly on the diffusion process in the Second Quarterly Progress Report. It consists of the following steps. We deposit a sputtered film of SiO_2 containing the dopant, usually zinc. A KMER layer is put on and a photo-mask is exposed. The KMER is developed by standard techniques, and the pattern of the doped SiO_2 film is produced by etching. The entire sample is then overlaid by another undoped, sputtered SiO_2 film. Finally, the sample is treated at 900°C in a hydrogen atmosphere to diffuse the dopant into the GaAs where the doped film still exists. Contact to the active areas may then be made by cutting windows into the SiO_2 film and using standard alloying techniques.

A series of diffusion runs was made to determine the junction depth found in diffusion from the doped SiO_2 film as a function of time. The experimental conditions are as follows. A zinc-doped SiO_2 film was sputtered onto a set of GaAs substrates. Diffusions were carried out for various times as indicated in Table IV. We see from these data that the sheet resistance, except for the very short diffusion run, remains constant from run to run. This indicates that only a certain specified quantity of zinc is diffusing out of the SiO_2 film during the diffusion, giving a Gaussian distribution for the deeper diffusions. Short diffusion times give the same junction depth, about 3 microns, regardless of diffusion time, because of the rapid diffusion concentration dependent behavior. Thus, we can control the diffusion depth very well without having to have a fine control of the diffusion time. To explain these data, (and some of the junction capacitance measurements described below), we theorize that the zinc distribution as a function of diffusion time and diffusion depth is that shown in Fig. 3. We think that for very short diffusion times the diffusion depth is exceedingly shallow, and the surface concentration is very high. In actual experiments, the zinc concentration is degenerate at the surface for short diffusions and tunnel diodes can be made from these layers. As diffusion time increases, the surface concentration decreases and the diffusion depth increases. This work is being further extended by studying the diffusion process using radioactive tracers. As the tracer work progresses, we will give quantitative results for the diffusions. A comprehensive review of the entire diffusion process will be written as a technical note.

TABLE IV

Diffusion from Doped SiO_2 Films

(900°C in H_2 Atmosphere)

Run	Time	Sheet Resistance (Ω/square)	Junction Depth (microns)
-94A	1 hr	33	3.0
-94B	30 min	38	3.0
-94C	15 min	46	2.5
-94D	64 hr	--	9.0
-94E	5 min	95	Couldn't measure, too thin

(Sheet resistances may not be valid because of thinness of layer and lack of precision of instrument.)

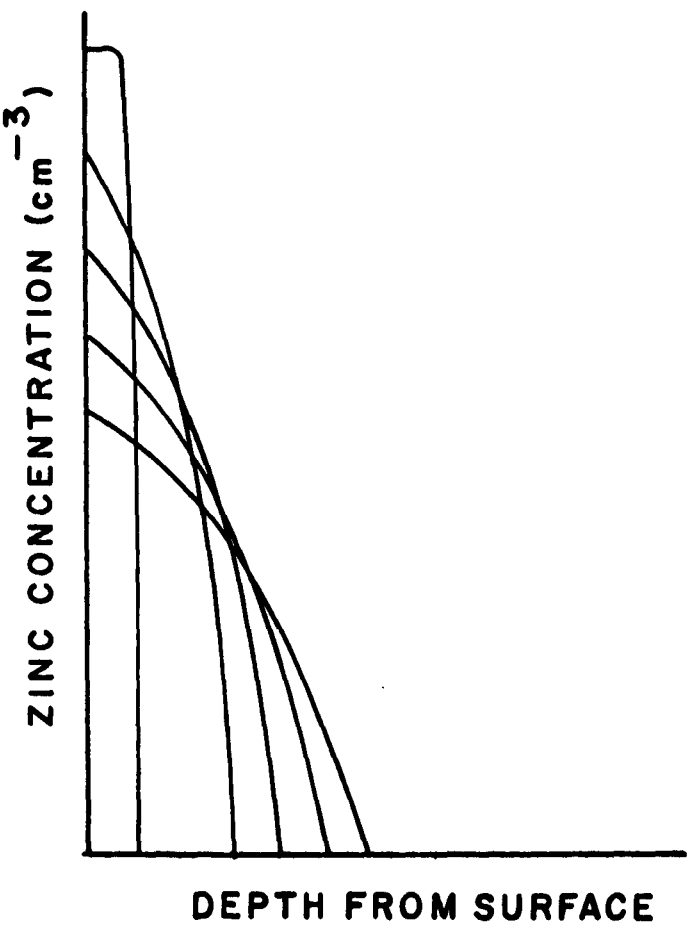


Fig. 3 Model of zinc diffusion in GaAs from SiO_2 film as a function of time. This model is used to explain diffusion data and junction capacitance measurements. Typically, short diffusions give surface concentrations as high as 10^{19} cm^{-3}. Note that the surface concentration decreases and the junction depth increases as diffusion time increases.

We have been studying junction capacitance as a means of determining some of the details of the diffusion process. The junction capacitance is the capacitance between the p- and n-layers caused by the application of a bias voltage between them. According to the diode equation:

$$C_j = A\,[V - V_d]^{-n} \quad ,$$

where C_j is the junction capacitance,
A is a constant,
V is the applied bias,
V_d is the contact potential, and
n is a constant for a given diode.

For an abrupt junction $n = 0.5$; for a graded junction $n = 0.33$. Determining the junction capacitance and in particular, the constant, n, allows us to determine the structure of the junction. The data plotted in Fig. 4 have been derived from junction capacitance measurements. In our original work the data were plotted by hand and the values read off from the curve. We have now written a computer program, and the results are obtained automatically.

We have used this method to study the difference between the old ampoule diffusion method and the newer doped SiO_2 film diffusion method. In the older method of diffusion, GaAs plus the dopant and sometimes some excess arsenic were sealed in an ampoule and diffused. Such a diffusion would have a step function impurity distribution, that is, an abrupt junction, because of the inherent nature of the diffusion method. The dependence of the junction capacitance on bias would approach the theoretical value of $n = 0.5$, indicating an abrupt junction. In our experiments several GaAs wafers with n-type impurities of about 10^{17}/cc were diffused for various lengths of time using the doped film method. For comparison a wafer was diffused in an ampoule with a metallic zinc source. In each case diodes were constructed from the diffused wafers and the capacitance measured as a function of applied voltage. The results are shown in Table V. The doped film diffusion indeed produces a junction whose capacitance-voltage dependence approaches the theoretical value of $n = 0.33$ (graded junction) as a function of time. These data are shown in Fig. 4, where we have plotted junction capacitance vs the difference in applied potential and contact potential.

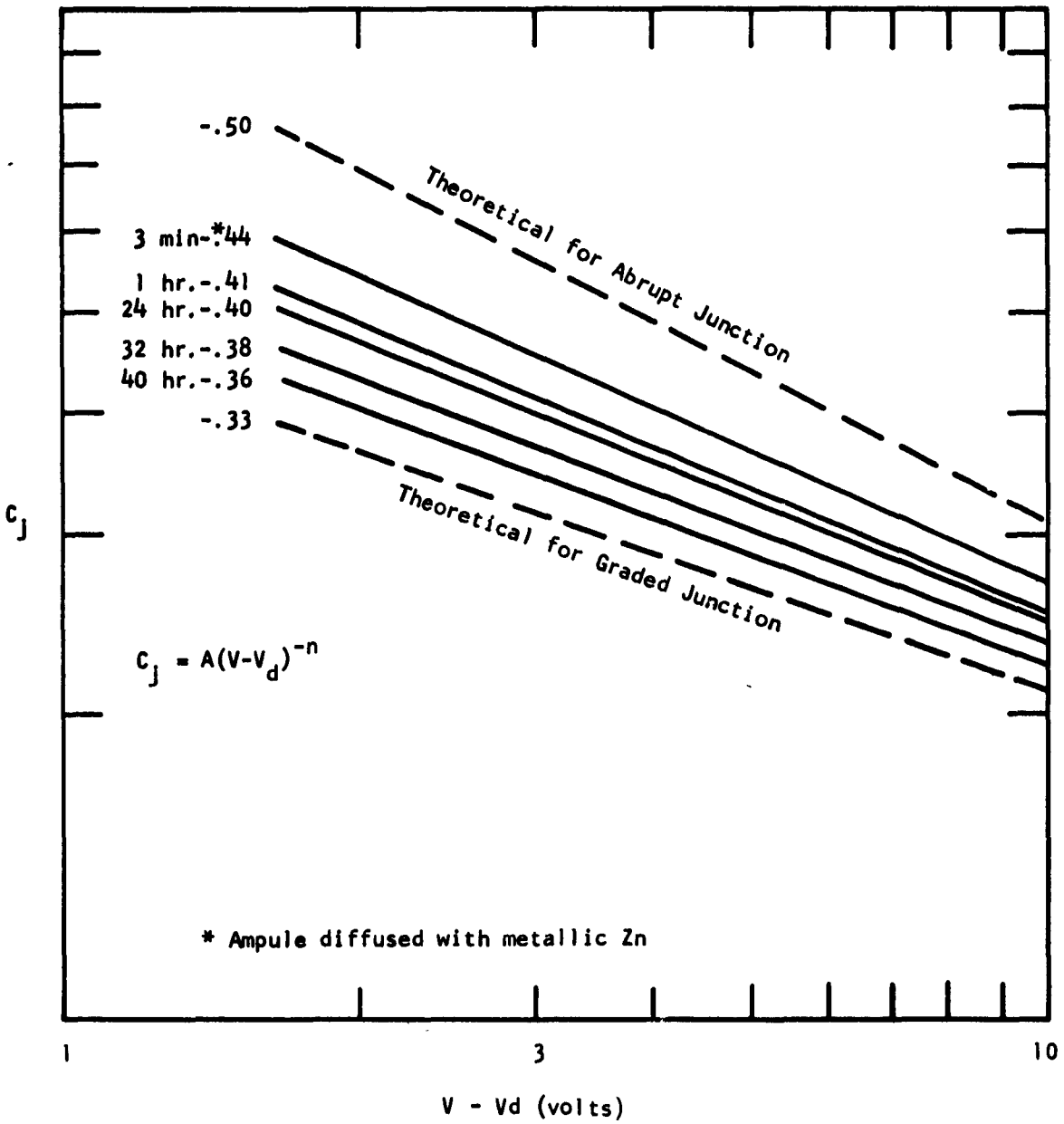


Fig. 4 Junction capacitance vs applied bias for diffused diodes. Except for the 3 minute diffusion, diffusions were made from doped SiO_2 films. Junction capacitance (C_j) was typically 100-200 pf; curves were normalized to indicate trend. Note that as diffusion time increases, slope approaches theoretical for graded junction.

TABLE V

Comparison of Diffusion Runs

Type of Diffusion	Time	n
Ampoule	3 min.	0.44
Doped Film	1 hr.	0.41
Doped Film	24 hr.	0.40
Doped Film	32 hr.	0.38
Doped Film	40 hr.	0.33

NOTE: n = 0.5 for abrupt junction, = 0.33 for graded junction.

With the understanding of the diffusion process gained through the work described above, we have been able to prepare diodes according to the scheme shown in Fig. 5 with minor variations. As indicated in the second quarterly report, the junction produced by this diffusion is exceedingly flat and well-behaved, and the diodes prepared in bulk GaAs show very low leakage and sharp breaking characteristics in the reversed direction. We made the first evaluation of the diffusion process on some of our epitaxial material during the third quarter. The epitaxial layer was approximately 20 microns thick. The diffusion was run at 900°C for 16 hours in a hydrogen atmosphere, and we estimated that the junction penetrated less than 10 microns. Thus, the junction is entirely within the epitaxial layer. Contact is made to the p-type material using Au-Zn alloy and to n-type material using Au-Sb alloy on a platinum tab. These diodes are not truly planar because the p-type regions were etched to a mesa-configuration. The diodes showed extremely good characteristics, with reverse breakdowns of more than 200 volts. Figure 6 shows the reverse and forward characteristics of two of these diodes. As mentioned above, these diodes demonstrate a basic problem in the electrical evaluation of epitaxial GaAs. The diode characteristics indicate very good material, i.e., a low carrier concentration. Hall effect and resistivity measurements indicate a medium purity material. We hope to resolve this dilemma with further work.

We have begun work on n-type diffusions to try to achieve a double diffused transistor structure in the epitaxial GaAs layer. We feel that it is important to use an all-diffused technology to take advantage of the best technologies available for completing this task. Most of the resistor and capacitor work, described in previous reports, was done with deposited metallic layers. We plan to produce these passive elements in a diffused structure as well.

Most of the GaAs transistor work, at TI and elsewhere, has been done on alloyed emitter, diffused base structures. We plan eventually to make a complex functional electronic block of GaAs containing many electronic components. For maximum packing density, diffusions using modern photomasking techniques will be necessary. Multiple emitter alloying operations will not be possible.

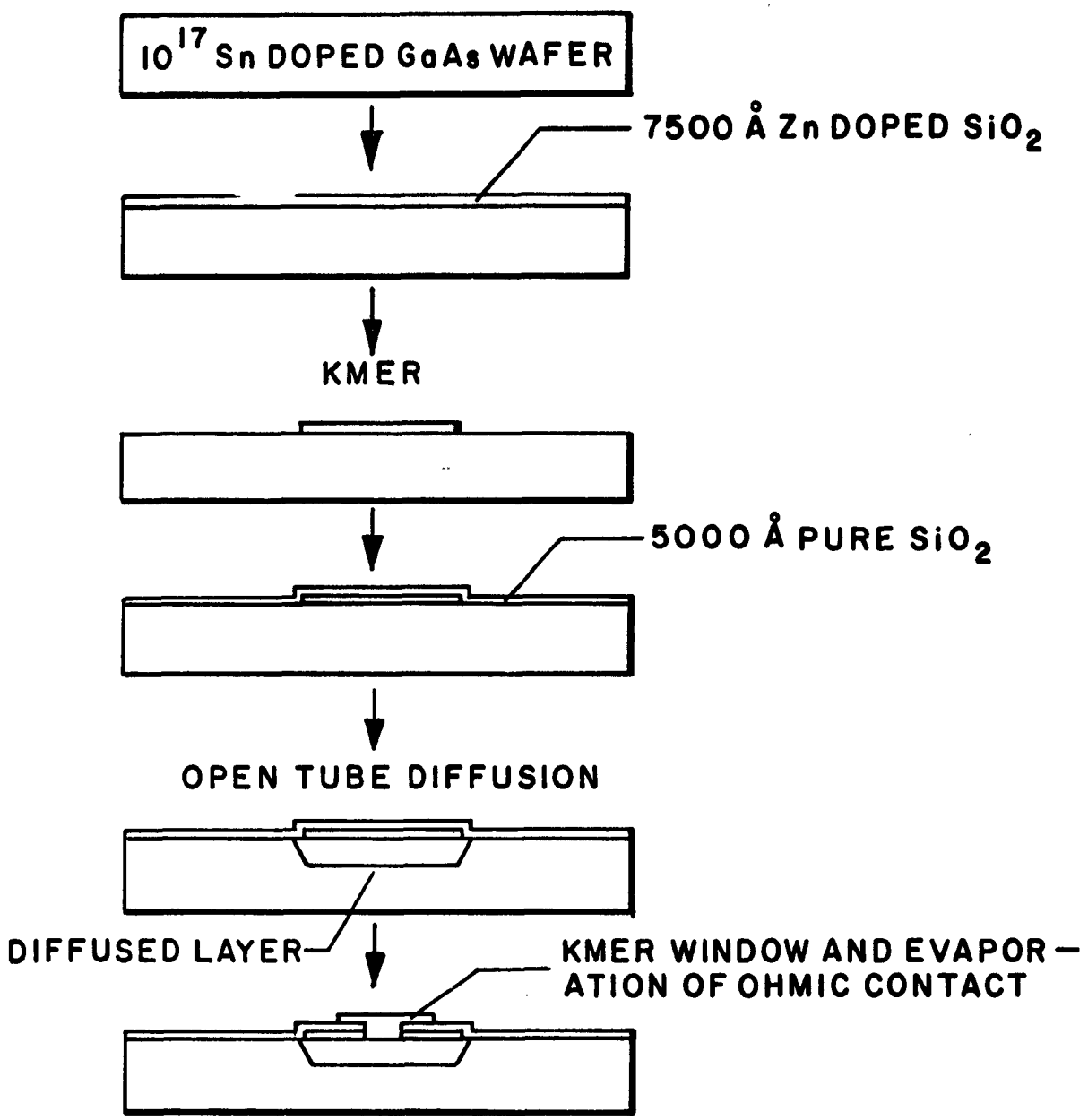


Fig. 5. Proposed system for preparing planar diodes by diffusion from doped SiO_2.

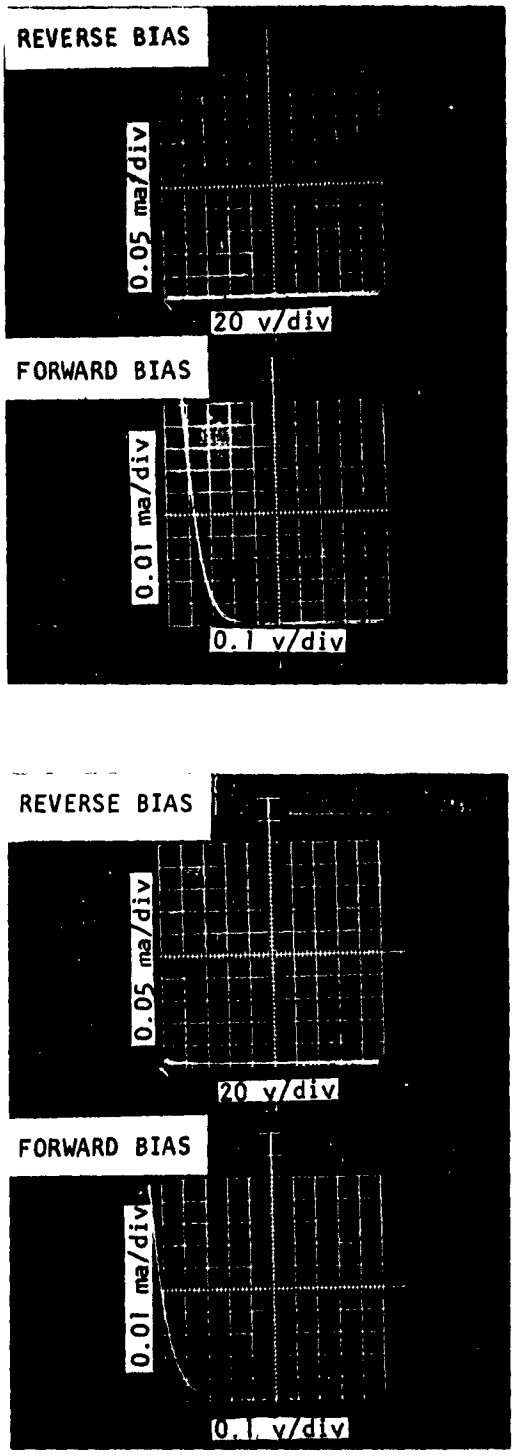


Fig. 6. I-V Characteristics of GaAs Diodes. These diodes have a diffused junction entirely within the epitaxial layer. Equivalent diodes made from the substrate show breakdowns of 10-20 volts.

In much of the silicon functional electronic block work resistors and capacitors have been made by depositing metal films on insulating layers on the silicon. This practice was necessary because electrical isolation in diffused circuit elements was impossible without reverse-biased junctions. Because of the problems of choosing proper bias levels for a number of components and the distributed capacitances, it is simpler and more practical to use evaporated layers. With the high resistivity substrate in the GaAs work, we will not have these problems and will be able to take advantage of the greater protection and stability of the diffused structure.

Earlier work with n-type impurities at TI and at other laboratories showed very poor results because of the chemical reactivity of the Group VI elements. During diffusion, wafers were eroded so severely that the surface loss rate, that is, the rate at which material disappeared from the surface, exceeded the rate at which the dopant diffused into the wafer. In some cases it was possible to dilute the dopant to reduce the reaction with the surface. However, under these conditions the surface concentration was not high enough to exceed the p-type carrier concentration. In addition, in the case of selenium, a surface layer of an amphorous glassy material forms which seems to have the composition of As_2Se_3. The surface layer ties up the arsenic and selenium and decreases the diffusion rate as well as attacking the surface.

We have been able to obtain normal diffusions with tellurium and good surface protection of the GaAs wafers by coating the wafers with a sputtered SiO_2 film. (Since our sputtering equipment for the tellurium-doped films has not been completed yet, initial work was done on wafers with an undoped SiO_2 film. The diffusion was carried out in sealed quartz ampoules with Te and Te-GaAs sources. The GaAs material was zinc doped to 10^{18} cc and sputtered on the B face with a 7000 Å SiO_2 film. When the new sputtering apparatus is available we will use it to produce tellurium-doped SiO_2 films.)

These exploratory ampoule diffusions were used to learn (1) if it is possible to obtain diffused layers without damage to the surface; (2) what doping levels can be expected in the surface; and (3) approximately what the diffusion coefficients are. Pure Te sources were used in some experiments,

and Te-GaAs sources were used in others. The alloy mixture was made by heating the reactants in a sealed ampoule at 1000°C for one hour to give 10% Te-90% As. Neither diffusion source showed a significant advantage over the other.

The junctions resulting from the diffusion were very smooth and regular. The GaAs used in this work was, of course, bulk GaAs and we expect to extend its use to epitaxial layers during the next quarter. Diffusion coefficients were calculated assuming an error function distribution of the tellurium in the GaAs. The experimental results are given in Table VI. Diodes were fabricated from the diffused wafers by etching mesas 5 x 5 mils. The reverse breakdown voltages were very sharp, and the reverse leakage was below the detectability limit of our apparatus, approximately 1 microampere. The higher reverse breakdown voltage seen for the 1100°C diffusion is assumed to be caused by an intrinsic layer in the material. Because the diffusions were made in a sealed ampoule with tellurium diffusing through the SiO_2 film, impurities may be introduced. We expect to have a better control of impurities when we begin depositing tellurium with the SiO_2 film. The voltage vs junction capacitance gave further evidence of an intrinsic layer. The diodes prepared from the 1000°C diffusion run showed a value of $n = 0.34$, which is the theoretical value for a graded impurity distribution. On the other hand, the 1100°C diffusion gave values from 0.177 to 0.248, which are below the theoretical limit and incapable of normal interpretation. These data cannot be explained in terms of a normal junction and could be the values found when an intrinsic layer appears in a junction.

We plan to extend these experiments to selenium. The diffusion coefficient reported for selenium seems to be high enough for our work, and the surface concentration, that is, the maximum solubility of the selenium in GaAs, seems high enough to yield a good emitter. Sulfur has been excluded as a possibility because its solubility, 1-2 x 10^{18}/cc, would not be high enough for our work.

TABLE VI

Te Diffusion Runs

	1000°C	1100°C
Surface concentration, Te, cm^{-3}	10^{19}	10^{19}
Zinc concentration, cm^{-3}	10^{18}	10^{18}
Junction Depth, microns	0.9	7
Diffusion time, hrs.	70	100
Diffusion coefficient	7×10^{-15}	3×10^{-13}
Diode voltage breakdown, volts	8	16

Using the diffusion process described above, we have attempted to make an n-p-n doubled diffused structure. The starting material was tin-doped GaAs at 10^{17}/cc. A zinc diffusion was carried out for 24 hours at 900°C using the SiO_2 film technique. The junction depth at this point was 3 microns, and the concentration vs depth for the impurities is shown in Fig. 7. The SiO_2 film was removed and a pure SiO_2 film, 7000 Å thick, was deposited. Tellurium was diffused through the film for 72 hours at 1100°C. The tellurium junction depth was then 5.5 microns, and the zinc junction depth had advanced under this heat treatment to 8 microns as shown in Fig. 7. No attempt was made to evaluate this transistor structure because the base width was too large and the original structure was not planned to have contacts. It may prove best to carry out the tellurium diffusion first, because of its lower diffusion coefficient. Under these conditions, then, the zinc would be diffused through the tellurium layer and would form a base layer in front of it. We plan to extend this work considerably during the next quarter.

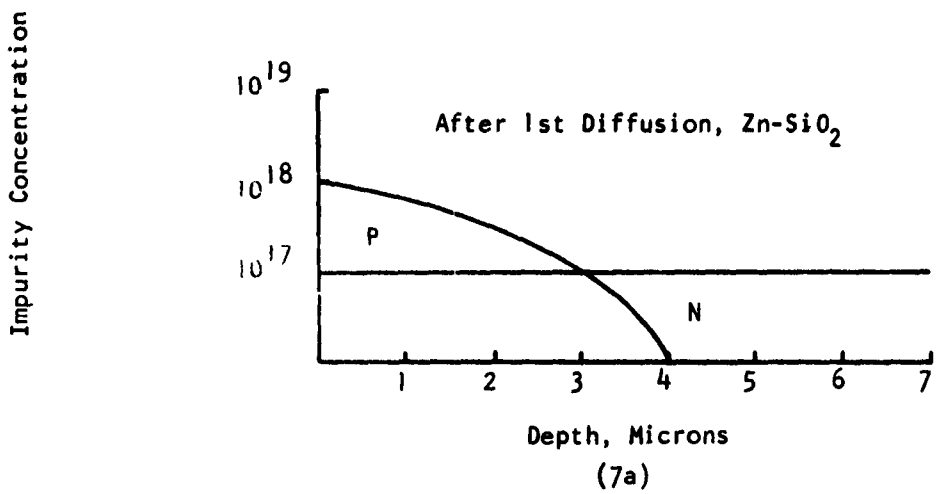
B. Task II--Three Dimensional Arrays

This task requires the production of epitaxial high resistivity GaAs layers which can be used to insulate circuit elements from each other vertically, while permitting vertical production of additional epitaxial layers. It is divided into two parts:

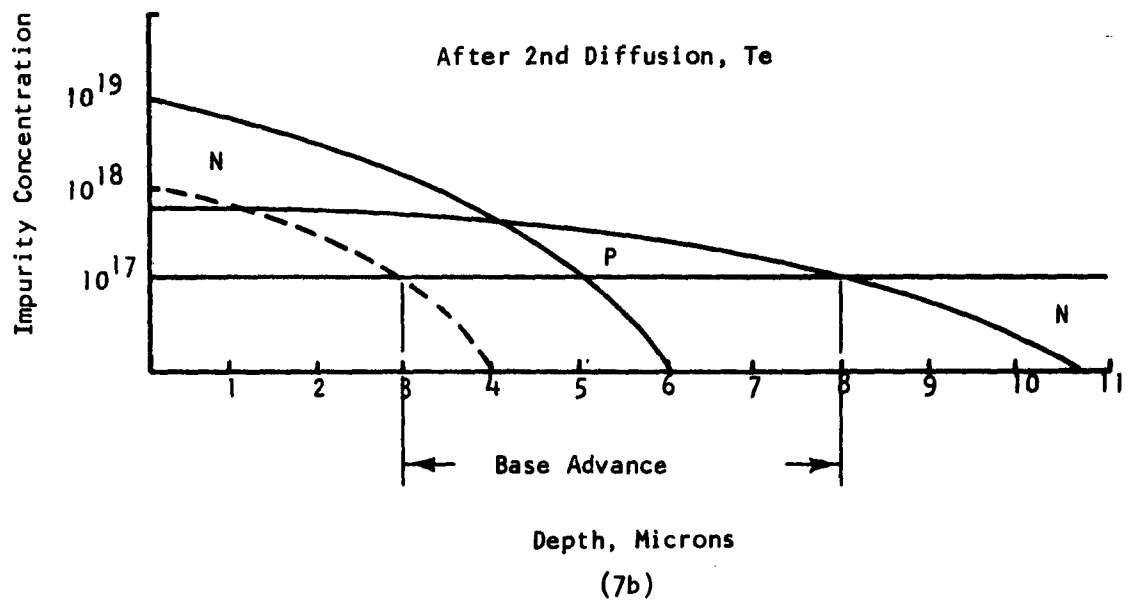
1. A study of methods to produce epitaxial high resistivity GaAs, and
2. Identification of the processes which cause breakdown between adjacent circuit elements separated by thin films of high resistivity material, so we might determine maximum packing density for functional electronic blocks.

Epitaxial Deposition of High Resistivity GaAs

We have continued work on depositing high resistivity GaAs using a closed bomb system with $AsCl_3$ as the carrier gas. No significant change in the deposition method has occurred since the details given in the last quarterly progress report.



(7a)



(7b)

Fig. 7 Double Diffused Structure in GaAs

In initial experiments this quarter, we tried to use zinc as a shallow acceptor and oxygen (as As_2O_3) as a deep donor to obtain high resistivity GaAs. The system has been proposed by Haisty, Mehal, and Stratton.[2] The formation of an oxide layer on the seed prevented deposition; the oxide layer is presumably due to the As_2O_3. These experiments were abandoned without further study of the system, since it seemed impossible to solve this problem. The next experiments were tried using GaAs feed material which contained zinc and oxygen. The material was p-type with carrier concentration of 10^{18}/cc. Runs with this feed material did not produce high resistivity epitaxial deposits. The deposits were p-type generally, with one n-type. In all cases the seed was oriented (111) with the GaAs deposited on the A face. These results are summarized (runs 1-4) in Table VII.

It seemed possible that the deposition process, that is, the time and temperature necessary for deposition, was causing thermal conversion of the seed or the epitaxial layer. We felt it wise at this time to run a series of experiments to determine if the resistivity and the electrical characteristics of the seed would change during the deposition process. It is very important to this process that the seed retain its electrical characteristics unchanged. Runs 5 through 10 in Table VII show the result of these experiments. The first attempt to deposit high resistivity GaAs in this series resulted in a p-type epitaxial layer about 80 microns thick. We were using low resistivity n-type seed for convenience. This same experiment was repeated using a high resistivity seed in the same feed material, time of deposition and other conditions being the same. After 16 hours, with a deposit of about 100 microns, both seed and deposit were p-type showing that there had been a change in the seed properties. In further runs in this series we noted that at lower deposition times, 2 or 4 hours, the electrical characteristics of the seed remained unchanged. For example, in run 8 a high resistivity seed remained high resistivity even though a deposit of 20 microns was built up on it in a period of 2 hours.

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[2] R. W. Haisty, E. W. Mehal, and R. Stratton, J. Phys. Chem. Solids 23, 829(1962).

TABLE VII

Epitaxial Depositions of GaAs - Closed System

Run No.	Seed Type	Source Type	Time (Hours)	After Deposition: Seed	After Deposition: Deposit (Type & Thickness)
1	Low, n	P-type (Zn + oxygen in GaAs)		n	p
2	Low, n	P-type (Zn + oxygen in GaAs)		n	p
3	Low, n	P-type (Zn + oxygen in GaAs)		n	p
4	Low, n	P-type (Zn + oxygen in GaAs)		n	n
5	Low, n	High Resistivity	16	n	p (80μ)
6	High Resistivity	High Resistivity	16	p	p (100μ)
7	Low, n	High Resistivity	2	n	n (20μ)
8	High Resistivity	High Resistivity	2	High Resistivity	n (20μ)
9	Low, n	High Resistivity (Zn + oxygen in GaAs)	4	n	No Deposit
10	Low, n	High Resistivity (Zn + oxygen in GaAs)	4	n	No Deposit

Source temperature, 800°C; Seed, 700°C; Carrier, $AsCl_3$. In runs 5-8 source material from accidentally produced high resistivity GaAs. In runs 9 and 10, zinc-plus-oxygen-doped GaAs used as source.

Having satisfied ourselves on this point, we then tried two runs using a zinc-plus-oxygen-doped high resistivity sample as the GaAs source. The results are shown in runs 9 and 10. In neither case did an appreciable deposit appear. The feed material had zinc in a concentration of approximately 2×10^{17}/cc. The oxygen concentration was not known but probably was considerably higher. It seems likely that in both runs an oxide film deposited on the substrate and prevented epitaxial deposition of the GaAs, as we noted in experiments using zinc-plus-oxygen separately.

Up to this time we had been using a piece of graphite in the deposition tube as a seed holder to establish a proper thermal gradient and other conditions necessary for best deposition of the epitaxial layer. Although we are working at much lower temperatures here than those usually found in the preparation of GaAs (800°C deposition temperature vs 1234°C melting point), there is some possibility that the GaAs seed or deposit is being doped by the graphite. A further series of runs listed in Table VIII seems to indicate that the graphite may be causing some of the trouble. It is noted that in all the runs in which graphite is used as a seed holder the deposit is n-type. We have also used a quartz seed holder which gives a physically poorer deposit (in some cases polycrystalline). We are now coating the graphite seed holder with SiC to prevent any graphite attack on the GaAs.

In addition to checking the possible uses of different seed holder materials, we have looked into a number of other methods of obtaining high resistivity GaAs. In Table VIII we have listed runs in which Fe-doped GaAs and Cr-doped GaAs are used as high resistivity source materials. In general, the results are not completely successful. There is some possibility that the Fe-doped material used with the quartz seed holder produces a high resistivity deposit.

Here, as noted previously under Task I, we are facing a big problem in evaluating the material. It is extremely difficult to determine the characteristics of a thin layer of GaAs deposited on the low resistivity seed. The

TABLE VIII

Deposition Runs - High Resistivity GaAs

GaAs Source	Seed Holder	Thickness (Microns)	Material Type
Undoped	Graphite	20	n
Chromium-doped	Graphite	20	n
Iron-doped	Graphite	20	n
Zinc + Oxygen	Graphite	20	n
Undoped	Quartz	Uneven, poly	n
Chromium-doped	Quartz	30	n
Iron-doped	Quartz	20	?
Zinc + Oxygen	Quartz	Uneven, poly	p

Source temperature, 800°C; Seed 700°C; Carrier, $AsCl_3$.
Deposition rate, 6 to 10 microns per hour.

system we have used tentatively in the past is to make point contact diodes to the layer and then attempt to determine the rectification properties of the point contacts at the surface. This system is unsatisfactory because it is too subjective and depends upon the interpretation of the operator. We plan to make alloyed tin contacts to the epitaxial layer to measure its properties more directly during the fourth quarter. The Semiconductor Physics branch of our Laboratory is currently concerned with many of these problems and will report on them in greater detail in the future.

High Resistivity GaAs Technology

In an appendix to the last quarterly progress report we covered in some detail the problems associated with voltage breakdown in high resistivity GaAs. The present discussion represents an interim report on samples we are examining in an attempt to understand the mechanisms of producing high resistivity GaAs and to understand limiting packing density and voltage breakdowns.

A crystal doped with both tin and iron (about 50 and 8 ppm, respectively) was obtained to back-dope to high resistivity with copper. We hoped to be able to look for the energy level of the iron by thermally stimulated emission measurements.

The original crystal was n-type with carriers ranging from 10^{14} to 10^{15}/cc in various parts. It had very low Hall mobilities, from 8 to 70 cm^2/V-sec. In the original crystal the conductivity as a function of temperature gave a slope 0.098 eV in the temperature range 140°K to 300°K. Thermally stimulated peaks were not obtained.

A sample was heated for six hours at 815°C and water quenched. It remained n-type, though its resistivity changed to about 100 ohm-cm. The sample was then diffused with Cu under the same conditions and converted to high resistivity p-type with 1.6×10^{11}/cc carriers. The resistivity was 9.3×10^5 ohm-cm and the mobility was 41 cm^2/V-sec, still low even for holes. The dark current vs temperature gave an activation energy of 0.55 eV. No thermally stimulated current peaks could be obtained over the temperature

range 77°K to 350°K. Similar results were obtained on material (10^4 ohm-cm) doped with Fe alone.

In the Second Quarterly Progress Report we discussed the necessity of determining the current-voltage curve of the material to understand something about its transport properties and voltage breakdown. We have an apparatus which can measure the current-voltage curves down to 77°K using currents small enough so the sample does not become heated. We have measured the current on a 0.35 mm thick sample of the Fe-doped high resistivity GaAs at low temperatures. The results are shown in Fig. 8. At low temperatures there was no breakdown up to 1600 volts. The behavior was not ohmic; current varied as $V^{1.5}$. At higher temperatures there was a break in the current-voltage curve, above which the current increased as rapidly as V^3, but the sharp breakdowns seen in other high resistivity GaAs never occurred.

For comparison with the iron samples we produced a sample containing chromium which is also high resistivity. The resistivity at room temperature is 1×10^8 ohm-cm and the mobility is 1100 cm^2/V-sec. Thermally stimulated emissions on this material showed traps at 0.28 eV and 0.42 eV. Figure 9 shows the current-voltage curves at room temperature and below. At room temperature there was no breakdown with increasing voltage up to 425 volts, when measurements had to be stopped because of excessive heating. As with Fe-doped GaAs, the current begins to increase as V^n where $n > 1$ at room temperature. The current in the chromium samples shows a $V^{3.5}$ dependence. (For space-charge-limited current, we expect the voltage coefficient, n, to be 2, and for the transition or breakdown at the traps-filled-limit voltage we have seen the coefficient very much larger than 3.5. It is not clear what causes this behavior.)

The way the current increases with time in this material seems to indicate we are filling several different kinds of traps at the same time and therefore see no abrupt transition from ohmic character to space-charge-limited current. Figure 10 shows current vs time for an applied voltage of 350 volts. The current is very small for 0.6 seconds and then increases

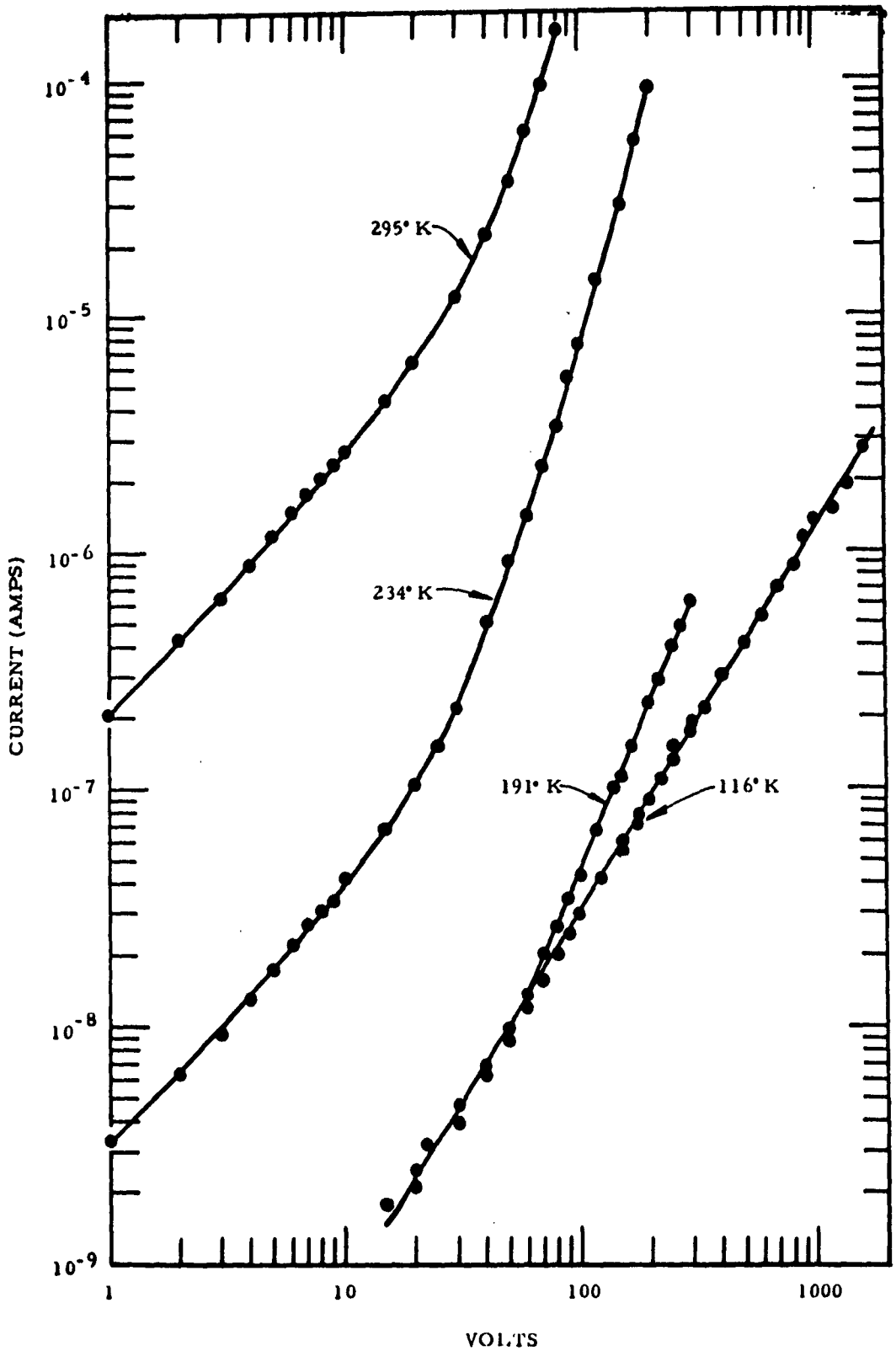

Fig. 8 Current vs voltage for Fe-doped high resistivity GaAs

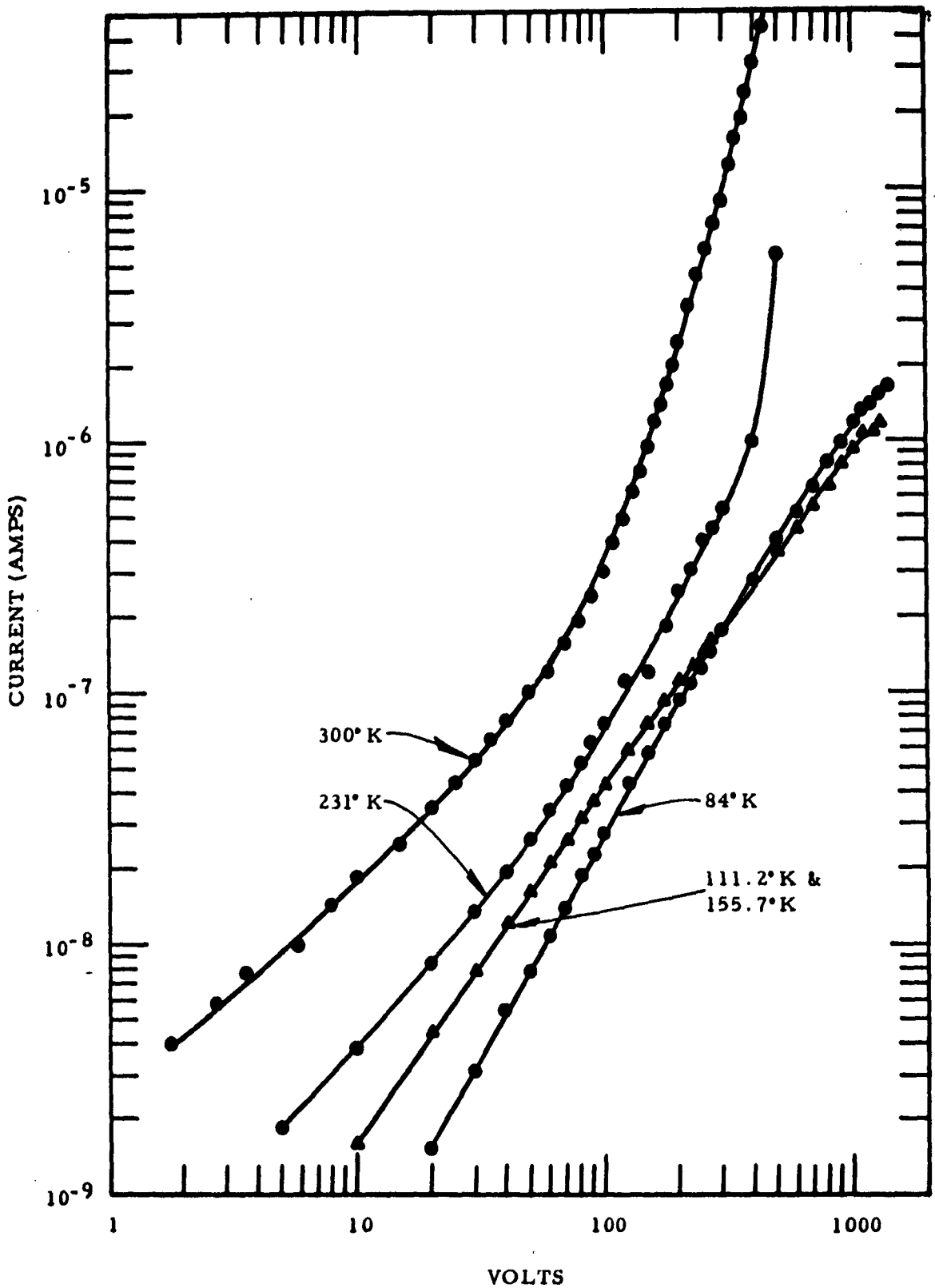

Fig. 9 Current vs voltage for Cr-doped high resistivity GaAs

Fig. 10 Current vs time in Cr-doped high resistivity GaAs at 230°K. Sweep: 0.2 sec/cm. Vertical: 2 μ amp/cm. The origin is 2 cm above and 4.2 cm to the left of center. Current is increasing in the negative direction. The initial spike is due to stray capacitance.

rapidly to a plateau, where it is delayed for 0.1 second. It continues to increase, finally going through several humps, then slowly decreases to an equilibrium value at about 10 seconds. These curves are completely reproducible except that the initial low current region varies with the length of time the current has been off. In Fig. 10 the current has been off about three minutes. When it is left off longer, the low current portion lasts longer, up to 15 seconds. This is evidence that during the low current portion, traps are filling and that these traps empty very slowly at this temperature, about 230°K. If the current is turned off and immediately back on, the low current portion lasts only milliseconds. Behavior of this material with hole injection contacts and as a function of thickness remains to be determined. However, we are encouraged because the resistance remained at approximately 10^7 ohms at 425 volts although the current had increased as $V^{3.5}$. (The sample was 0.54 mm thick.) We are also encouraged in using the Fe-doped GaAs as an insulating substrate from the standpoint of voltage breakdown and ease of preparation. It has a reasonably high resistivity. The complete absence of thermally stimulated peaks in this material is very interesting, particularly since a peak at about 0.15 eV, associated with copper, has appeared in all other high resistivity material we have measured except the Cr-doped material.

We are still not certain that the current in these high resistivity samples and across very thin layers can be described properly by the theories currently in vogue. In particular, the low voltages at which the transition to space-charge-limited current occurs (with In or Sn contacts) give values less than 10^{13}/cc for empty trap concentrations, which is in great contrast to trap concentrations of 10^{17}/cc or higher found from thermally stimulated emission measurements. Two possibilities exist: (1) the electron traps are actually present only in small amounts, the high trap concentrations being all hole traps; or (2) the breakdown is not adequately explained by the space-charge-limited current theory.

In an experiment to check the first possibility we found that a 0.1 mm thick sample with Sn alloyed contacts broke down reversibly at 20 volts, while a similar sample with Zn diffused contacts did not break down until 200 volts. At that point the breakdown was permanent; that is, an irreversible change took place. This large difference in breakdown voltage is in agreement with the first hypothesis above.

To check the second point, a sample with electron injecting contacts (indium) was successively lapped thinner and thinner. It was measured after each lapping to determine whether the breakdown voltage varied as the square of the sample thickness as theory predicts. From 0.16 to 0.3 mm the voltage did vary as T^2. From 0.3 to 0.8 mm, the variation was less steep, about $T^{1.3}$. At 0.95 mm the breakdown did not occur at 1200 volts, the maximum available to us then. A new apparatus is now available to go to 30 kv and has been tested by the operator at 12.5 kv. Possibly the breakdown in very thin samples is explained sufficiently by the space-charge-limited current theory. For intermediate thicknesses, a second process is involved.

This may require a critical density of injected carriers in a critical field. In any case, the failure to break down at 0.95 mm is puzzling. The results of these experiments tell us that electron traps are needed to increase the breakdown voltage for electron injection. Part of our research program will be concerned with making or finding high resistivity GaAs with electron traps as determined by measuring the sign of the Hall voltage during thermally stimulated emission. We will use such material for breakdown measurements as a function of thickness and further experiments.

C. Task III--II-VI Photo Effect Devices

We are primarily concerned in this task with devices made from CdS. Our efforts have been toward improving the purity and electrical characteristics of the material as well as producing large single crystal ingots to make into devices. During this report period we began supplying CdS for use on contract AF 33(657)-9824, work being done in TI's Networks department.

Materials and General Technology

In the previous quarterly progress report we described the techniques used to produce the CdS used in this work. In the third quarter we improved the purity of the material and gained better control of the doping concentrations of Cu and Ag used to achieve the necessary high resistivity. The purity of the material seems to be under good control, as indicated by the data in Table IX. To some extent Zn and Pb still plague us with random appearances which do not correlate with any other experimental evidence to show why they should be there. Some minor amounts of other impurities appear from time to time, but in general, the ingots of CdS show very good purity.

Various doping agents and experimental conditions for material preparation have been tried in various runs. For example, indium-doped runs, Nos. 17-1 and 20-2, have been prepared for use in the Networks department. We tried Ag-doping in runs 11-2 and 15-2 to compare that material with the Cu-doped material. The characteristics of some of these samples are shown in Table X, where the resistivities in dark and in light are given. In addition, run 19-2 was made with an atmosphere of H_2S. Initial results indicate that sulfur vacancies may help explain our low resistivity problems in undoped and acceptor type impurity crystals. Although the crystal yield was not extremely high resistance, a trend toward high resistivity from the established norm is observed, strongly suggesting that this line of research should be followed up.

The Ag-doped CdS runs are interesting as a source of high resistivity CdS other than Cu-doped. The material is quite uniform and shows good luminescence properties. We can cover the range of concentrations of Ag in CdS from about 50 ppm to more than 5000 ppm. The dark resistivity is about 10^6 ohm-cm, which is not quite high enough. Further work may be necessary on this system.

Much of the work during this period has gone into a study of the shallow diffusion of indium into CdS to produce a surface layer with properties necessary for device formation. This work is being submitted to ASD

TABLE IX

Spectrographic Analyses of Typical Crystals

SPECIMEN DESCRIPTION	IMPURITIES (ppm)															
	Si	Pb	Mg	Cu	Zn	Ca	Na	Mn	Sn	Fe	Cr	Al	B	Ag	K	In
Minimum Detectable Levels	<0.3	<1.0	<0.01	<0.1	<100	<0.3	<1.0	<0.1	<0.5	<1.0	<2.0	<2.0	<0.5	<0.2	<1.0	
Starting Material Lot 135	1.5	17	0.27			0.15										
Run 88-1* Cu-doped	0.85		0.065	14.5												
Run 10-2* Cu-doped	3.3	1.0	0.75	7.8	10	1.4	4.0	<0.05		3.6		3.6	<0.05	0.04		
Run 11-2 Ag-doped ($AgNO_3$)	0.88	0.8	0.17											150		
Run 12-1 Cu-doped			0.19	2.2												
Run 13-1 Cu-doped	0.44	2.0	0.37	2.2										0.45		
Run 14-1* Cu-doped	0.32		0.35	9.4	34	<0.1	1.5			<0.5				1.04		
Run 15-2 Ag-doped ($AgNO_3$)	3.9		0.5	1.8	70	3	3			<0.5				1500		
Run 16-1 Cu-doped (Cu_2S)	1.9		2.4	8.6												
Run 17-1 (Indium Doped)	10-100		0.98	16						11				3.7		0.5-5.0%
Run 18-1 (Cu Doped-CuS)	ND to 4.5	ND to 61.0	0.69 to 2.6	25.5 to 33.2						ND to 3.3						
Run 19-2 (H_2S Grown)	2.05 to 5.1		1.9 to 5.9	0.59 to 11.6				ND to 0.43		ND to 5.5				0.09 to 0.49		
Run 20-2 (Indium Doped)	5.3 to 6.3	ND to 15	0.5 to 0.69	2.1 to 2.7						ND to 1.1				0.12 to 0.30		0.5%

< = Less than

ND = Present, if at all, in concentrations less than the minimum detectable.

* Indicates different starting material

All Cu-doped runs used Cu metal powder 300 mesh except 16-1, in which Cu_2S was used in an effort to offset possible stoichiometry effects (sulfur deficiency).

TABLE X

Resistivity of Typical Crystals as a Function of Light Intensity

Run	Dopant[+]	Dopant Conc. (ppm)	Resistivity (ohm-cm)		
			Dark	Medium Light (~50 ft-C)	High Light (~1000 ft-C)
17-1	In	0.5-5.0%	0.005	0.005	0.005
18-1	Cu	25.5-33.2	2.4×10^{10}	1.05×10^{8}	7.7×10^{6}
19-2	*		?	6K-60K**	200K-1M**
20-2	In	ND	4	4	4
21-1	Cu	?	6.7×10^{6}	2.34×10^{3}	150

[+] Dopant - an intentionally added impurity.

* Not intentionally doped.

? Data unavailable at this time.

** Tentative data.

as a technical note. We have shown the feasibility of using In vapor diffusion at relatively low temperatures, 500°C for 10 to 20 minutes, to produce light transparent conducting channels and photosensitive electrically isolated islands on the surface of high resistivity CdS substrates. In addition, we have demonstrated the use of Al as a mask to outline the surface areas in the diffusion. Electrical and visual evaluation of numerous diffusion runs has provided the critical techniques necessary to fabricate the functional electronic block circuit elements. With this In diffusion technique we have been able to solve the problem of connecting circuit elements prepared on the surface of a CdS single crystal.

Our work on making diodic contacts to CdS has mainly involved the use of tellurium, as reported previously. In particular, we have considered using tellurium on the indium diffused surface to give a diode action. These contacts have had uniform but very poor characteristics. The rectification ratio usually seen is about 10 to 1, and the nominal reverse breakdowns have been less than 100 volts. (The rectification ratio is the ratio of current carried in the forward direction for a few volts bias compared to the current carried in the reverse direction for the same bias in the reverse direction.) Since the diodic contacts are important for any devices we hope to build from CdS, we have studied them in some detail.

Further work has shown that the rectification ratio of the tellurium contact can be improved by simultaneously applying heat and an electrical field at temperatures up to 300°C and with electrical biases to 200 volts. The improvement ratio is limited so far to a maximum of an order of magnitude, that is, from approximately 10:1 to 100:1. It has been found that the as-formed fused tellurium electrodes may be either anodic or cathodic with respect to the indium diffused surface on the CdS. Furthermore, the tellurium is apparently changed back and forth at will, depending on the direction of the electric field when it is applied at an elevated temperature. This leads us to believe that the changeable barriers are the controlling factor in this particular contact. Thus, there is not a simple injection of carriers into the CdS. Instead, a Schottky-type barrier may be determining the characteristics of the contact. On the basis of this work we are re-examining the indium contacts on other samples which have had the indium surface treatment. It was

found that they also could be made to exhibit somewhat changeable rectifying characteristics rather than the assumed linear ohmic behavior we have seen before. This further strengthens our belief in the barrier model in this particular case. The changing character of these contacts does not invalidate their use as electrical connections, as mentioned above. The low resistivity of the indium layer compared with the resistance of the base CdS allows the indium diffusion treatment to achieve its goal. In general, the contact work outlined here is indicative of the type of problems we are having with all contacts to the CdS. We hope to be able to solve these contact difficulties in the remaining period of the contract.

Devices

Device work has been delayed because of our need for a better contact technology. Furthermore, in discussions with the contracting agency it has become apparent that this work is less important than the rest of the contract work. However, a considerable amount of work has been done on a photocapacitor made of CdS. In particular, an exhaustive analysis has been made of the capacitance change that might be expected as a function of the light intensity. This comprehensive work is presented in this report as an appendix.

During the third quarter we have increased our capability in some of the measurement techniques. We found it necessary to set up a special apparatus for testing the diodes in connection with the contact work, and we have begun to measure some of the piezoelectric resonances found in the CdS samples we have been working with.

D. Task IV--GaAsP and GaP for Epitaxial Devices

In the work originally proposed under this task we were to produce GaAsP and GaP by two methods. In the first method we attempted to diffuse phosphorus into GaAs in a sealed tube, thereby giving a graded composition from GaAs in the bulk to GaP in the surface. In the second method of

preparation we attempted to produce an epitaxial deposit of the desired composition from the vapor phase, much as we are doing in epitaxial GaAs deposition. At the end of last quarter's work we decided that diffusing phosphorus into the GaAs would not produce the type of layers which would be useful in further device work. The layers were misoriented and sometimes polycrystalline; they showed a discontinuity in properties between the layer and the bulk GaAs. In addition, it was extremely difficult to produce a layer which did not show the effect of oxygen contamination. Therefore, no work was done on this subtask during the third quarter. Instead, emphasis was on epitaxial deposition.

Work on depositing GaAsP or GaP on GaAs substrates has been directed along the following lines:

1. To extend the range of compositions available to us over the complete range from GaAs to GaP;
2. To produce purer deposits, that is, to get a better control of the purity of the starting material and the deposition conditions;
3. To develop a new reactor system or apparatus to allow us to produce thicker deposits and to get a better control of the surface features and physical character of the deposit;
4. To learn how to control doping to a concentration required for device technology or to achieve characteristics desired in the material;
5. To solve the problem of the deposits physically fracturing from the seed, particularly in the cases of the higher phosphorus concentration materials.

During the third quarter we extended the range of composition of the deposition to include all compositions between GaAs and GaP. Table XI shows the runs in which there was no change in composition of the deposited layer during the time of the run. It should be noted from Table XI that we have extended our range of experimental conditions markedly in the last quarter.

TABLE XI

Epitaxial Depositions of $GaAs_xP_{(1-x)}$

Run No.	Source and Source Temperature °C	Seed Temperature °C	Flow Rate - cc/min. PCl_3	Flow Rate - cc/min. $AsCl_3$	Flow Rate - cc/min. H_2	Time (hrs)	Remarks
734-58	GaAs 915	790	4	0	192	4.0	176μ deposit.
-60	GaAs 915	800	4	0	192	3.0	Results same as -58.
-61	GaAs 915	790	4	0	192	2.5	Furnace leak, no deposit.
-62	GaAs 915	800	4	0	192	4.0	Recheck of temperature profile.
-63	Ga 925	795 to 600	7	0	192	3.8	225μ deposit. Single even at 600°C.
-64	Ga 950	750 to 550	9 to 34	0	155	4.3	Turned poly in high PCl_3 flow.
-65	GaAs 915	790	4	0	192	3.5	$GaAs_{0.6}P_{0.4}$ on high resistivity.
-66	GaAs 915	790	4	0	192	3.5	$1 \times 10^{20} cm^{-3}$ zinc-doped source.
-68	GaAs 915	790 to 760	4	0	150	3.5	$GaAs_{0.6}P_{0.4}$ for device use.
-70	Ga 950	790	4	42	110	5.0	2 seeds, both $GaAs_{0.5}P_{0.5}$.
-71	Ga 950	790	4	20	110	4.5	130μ, $GaAs_{0.37}P_{0.63}$.
-73	Ga 950	790	1	42	110	4.0	$GaAs_{0.8}P_{0.2}$ highly doped
-75	GaAs 920	800	5	0	173	4.0	Polycrystalline

GaAsP materials are being deposited using both GaAs and elemental Ga as the source material and either PCl_3 or a mixture of PCl_3 and $AsCl_3$ as the vapor-carrying gas and source of phosphorus. We were able to achieve much thicker deposits, as much as approximately 0.01 inch. To some extent the depositions reported on in Table XI represent attempts to produce material on order for the use of the Networks department in Texas Instruments for work on Contract No. AF 33(657)-9842.

Our success in obtaining the thicker deposits and the wider range of experimental conditions has depended in part on a new deposition reactor which we started using during the quarter. The reactor is identical to the one described in the last quarterly progress report for use on GaAs. Its flexibility has allowed us to use Ga as a source material and to deposit much thicker layers. We can summarize our materials preparation efforts as follows:

1. Material composition of the deposited layer can be made for $GaAs_xP_{(1-x)}$ for any desired value of x.
2. Single crystal deposits up to 225 microns (0.009 inch) and deposition rates up to 60 microns/hour are possible.
3. Some preliminary attempts have been made to produce doped layers containing zinc.

As noted in the monthly reports, one of our problems has been that GaP layers or layers rich in phosphorus have physically fractured from the substrate. The fracturing is caused by a lattice mismatch between the GaAs seed and the deposit or by a difference in the thermal coefficients of expansion. The problem has been solved by depositing a thin intermediate layer of a composition between GaAs and GaP and then changing the system to deposit GaP. In Table XII we list some of the runs during which the composition of deposit changes. In particular, run 734-74 shows the conditions necessary to deposit a thin intermediate layer of $GaAs_{0.6}P_{0.4}$ and then a GaP layer on top. The GaP layer produced in this way adheres very well to the GaAs seed and shows no signs of physically fracturing.

TABLE XII

Epitaxial $GaAs_xP_{(1-x)}$ Deposition Runs

(Variable Composition)

Run #	Feed Temp °C	Seed Temp °C	Total Hydrogen cc/min	PCl_3 Bubbler cc/min	$AsCl_3$ Bubbler cc/min	Time hrs	Remarks
R734-72	950	790	110	2 ↓ 4	42 ↓ 20	2.0 2.0	Single surface, but grew in many layers. 350μ thick
R734-74	950	790	110 ↓ 138	2 ↓ 7	30 ↓ 0	20 min ↓ 4.0	Excellent transition from $GaAs_{.6}P_{.4}$ to GaP
R734-76	950	790	110	1 ↓ 3	33 ↓ 0	1.0 1.0	GaAs-$GaAs_{.7}P_{.3}$-GaP

Note: An arrow indicates a change in composition or conditions during the run. See text for further details.

Attempts to produce a purer deposit have primarily involved purifying the PCl_3. (Our $AsCl_3$ is very pure, coming from a distilled product from a Texas Instruments line used to produce arsenic by hydrogen reduction.) Table XIII shows the mass spectrographic analysis performed after we have distilled the PCl_3. This PCl_3 is now used routinely in all depositions, and we have achieved a GaAsP which shows relatively good characteristics. The composition was $GaAs_{0.6}P_{0.4}$, grown on a high resistivity GaAs seed. We assumed contacts made to the epitaxial deposit were ohmic and showed the characteristics of the epitaxial layer only. Carriers were 3×10^{16}/cc, and the Hall mobility was 1750 cm^2/V-sec at 300°K. This sample shows a decreased donor concentration and increased mobility compared to previous samples. These results, however, are not a complete evaluation of the new PCl_3 because the feed material used in this particular deposition was GaAs with a donor concentration of 2×10^{16}/cc. This latter factor probably diluted the purity of the deposit. We should be able to deposit still purer material with better feed material. We have not tried to push our purity beyond this point because of the press of other things.

To extend the range of compositions and in particular, to make doped material, we have tried depositing doped GaAs, usually of a $GaAs_{0.6}P_{0.4}$ composition. Because the material produced without intentional doping is n-type, we have concentrated on p-type dopes. In the first case we used GaAs feed material that had been doped with manganese. The manganese was vapor carried in the deposition system as it should have been, but the deposits were polycrystalline p-type. In further experiments cadmium was mixed physically with the GaAs feed material and used as a source in the vapor deposition. In two experiments with cadmium the deposits were single crystalline and medium to high resistivity p-type. In two further experiments with zinc physically mixed with GaAs, the deposits were single crystalline and low resistivity p-type. In all cases the substrate was originally low resistivity n-type, and in the cadmium and zinc experiments there is some indication that the substrate had gone to a higher resistivity, that is, started to convert thermally to p-type. This is a problem which we have not yet been able to

TABLE XIII

Mass Spectrographic Analysis of PCl_3

	As-Received	After Distillation
Major	PCl_3, PCl_2, PCl	PCl_3, PCl_2, PCl
3-5%	$POCl_3$, $POCl_2$, etc.	
~ 1%	HCl, PH_3, P, Cl	HCl, P, Cl
Trace	CCl, C_2H_5, CH_3, O, OH, H_2O	C, CH_2, CH_3, OH

Note: Fracturing of PCl_3 will produce, PCl_2, PCl, P and Cl in analysis

solve. In another experiment using zinc doping we started with a GaAs feed material containing about 10^{20}/cc zinc. Although the deposit of $GaAs_{0.6}P_{0.4}$ was single and p-type, not enough zinc had transferred to give a degenerate deposit. This latter experiment was made to determine the upper limit of the zinc doping we could achieve using this method.

One problem area remains in the deposition of two or more compositions of GaAsP or GaP. Run 734-72 showed this problem to some extent. This run was an attempt to deposit two compositions on the GaAs seed and was produced as follows. A deposit was grown for two hours under conditions that would produce $GaAs_{0.67}P_{0.33}$. The conditions were then changed to grow a more phosphorus-rich composition, $GaAs_{0.33}P_{0.67}$, for two more hours. The result was a peculiar multi-layer deposit with many more interfaces than could be accounted for by deliberate changes in run conditions. These interfaces were visible when a cross-sectional examination of the layer was made under a microscope. They showed up in the deposited layer as dark lines running roughly parallel to the original surface of the seed. These layers seemed to be caused by either a growth rate that was too rapid (78 microns per hour) or a composition change that was too abrupt. In another run, 734-76, we attempted a slower growth rate but a more abrupt composition change. A $GaAs_{0.7}P_{0.3}$ composition was grown for an hour; then the composition was changed to GaP, and a 30 micron per hour growth rate was maintained for another hour. The resulting deposit had an excellent interface between the seed and the first deposit and a relatively good interface between the first and second deposits. This shows that the peculiar multi-layer structure of the previous run was probably caused by too rapid a growth rate. However, the interface between the two deposited layers shows irregularities generated by the growth of the first layer. That is, if care is not taken in depositing the first layer, any irregularities grown on it will show up in the interface between that layer and the new composition layer deposited on it. When a single deposit is made, the surface growth facets are easily removed by lapping before the material is used. However, the interface between deposits of graded compositions of material cannot be physically treated before a new composition is deposited on it. Thus, we may have an uneven interface

across the crystal. Some reliable method for growing deposits with very smooth, even surfaces seems more necessary here for continued graded composition work than in the epitaxial GaAs work. All results of this work on smooth deposit interfaces will, of course, be applicable to the three-dimensional layer work being done under Task II.

III. PLANS FOR NEXT PERIOD

TASK I

1. Extend device work to produce transistors and passive elements in epitaxial GaAs.

2. Determine conditions necessary to produce doped epitaxial layers, both n- and p-type.

3. Finish design on a simple FEB in epitaxial GaAs and construct prototype.

TASK II

1. Deposit doped GaAs layers of high resistivity material.

2. Continue study of high resistivity mechanisms.

TASK III

1. Continue studies on contacts.

2. When contact work is sufficiently advanced, prepare a simple circuit employing photo-variable diodes.

TASK IV

1. Prepare doped GaAsP deposits to specification.

2. Resolve difficulties experienced in depositing multilayers.

IV. PERCENT COMPLETION

This contract is 62% complete.

APPENDIX A

PHOTOCAPACITOR STUDY

Y. T. Sihvonen, D. R. Boyd, E. L. Kitts

PHOTOCAPACITOR STUDY

Y.T. Sihvonen, D.R. Boyd, E.L. Kitts

INTRODUCTION

Sufficient technology is now at hand to fabricate single crystal CdS light sensitive capacitors, which are operationally simple enough to be interpretable with analytical methods. Earlier units, because of their complex geometry, pointed up certain problems that not only prevented optimum device performance, but also prevented gaining insight into the basic mechanisms involved. Generally speaking, these problems involved (a) ascertaining relative roles played by the CdS dielectric and the depletion layers introduced by the tellurium contacts, (b) the diodic contacts formed by the tellurium contacts, and (c) getting light into the bulk of the device through the contacts. Specifically, these problems are depicted in Fig. 1.

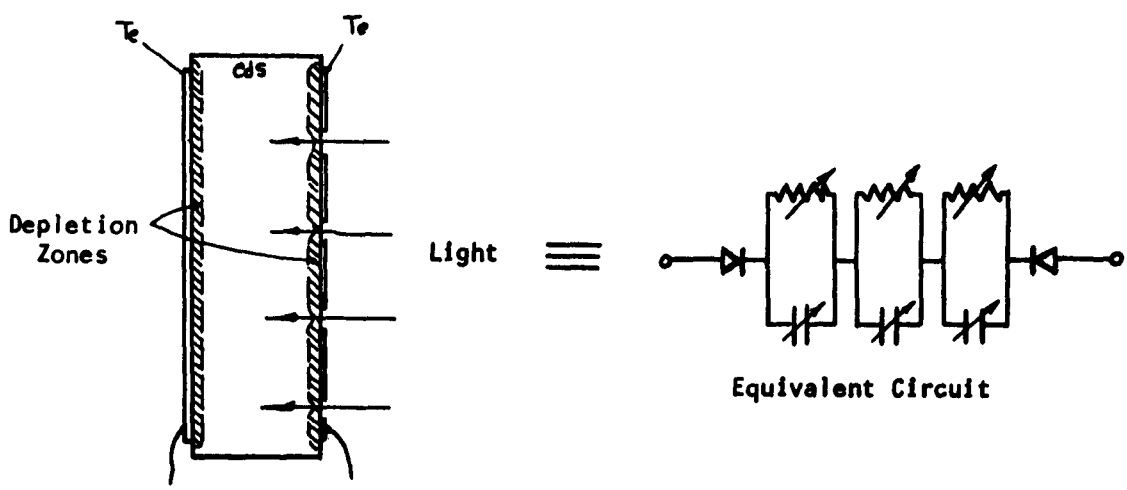

Fig. 1

Our first units were fabricated by evaporating tellurium contacts onto the broad faces of a CdS slice with suitable apertures in one contact to allow

light to enter into the bulk of the device. While these units showed photocapacitance effects, basic insight was obscured because of the influences of conducting channels introduced into CdS dielectric, coupled with the existence of three dielectric media between contacts (CdS bulk plus two depletion zones), and further complicated by the diodic contacts that alternately shifted capacitance effects from one contact to the other under ac field excitation.

With the successful preparation of CdS materials and their processing into desirable shapes together with appropriate masking and indium-diffused islands, we are now prepared to make a definitive experiment. This report details the analysis of the problem and progress to date.

FABRICATION DETAILS

Figure 2 depicts the photocapacitor as it has been constructed for study. A high dark resistivity photosensitive CdS slice is masked with evaporated aluminum and heated in the presence of indium vapor at 550°C for 15 minutes. The indium diffuses into the CdS surface through a circular

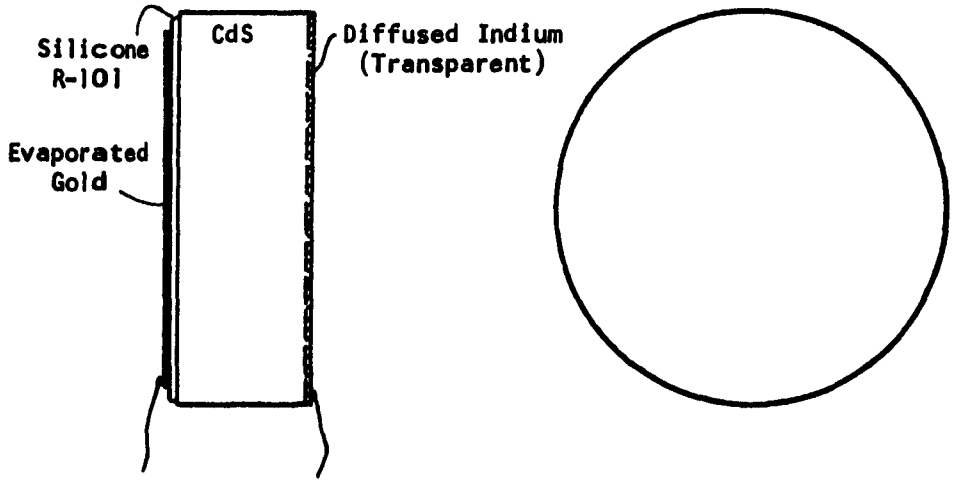

Fig. 2

aperture in one mask, and forms a low resistance transparent ohmic contact which serves both as a light window and one plate of the capacitor (in the dark). The aluminum mask is etched off with NaOH, after which an insulating film of Silicone R-101 (Union Carbide) is cured onto the opposing crystal surface. The second capacitor plate (gold) is then evaporated onto the insulating film directly opposite from the transparent indium contact. The resulting device consists of a parallel plate capacitor with two dielectrics, one of which is photoconducting. Light enters the system through one contact, which is ohmic and transparent, and forms a conducting medium that parallels the contacts. The front of this conducting medium is effectively a moveable capacitor plate and is controlled by the wavelength of the incident radiation.

Ultimately, the silicone dielectric will be replaced by a high resistivity depletion layer on the CdS surface. But for this first series of tests it is desirable not to include a depletion layer, since it introduces one additional degree of complexity in the analysis.

ANALYSIS OF PHOTOCAPACITOR PERFORMANCE

Figure 3 depicts the photocapacitor and its electrical equivalent

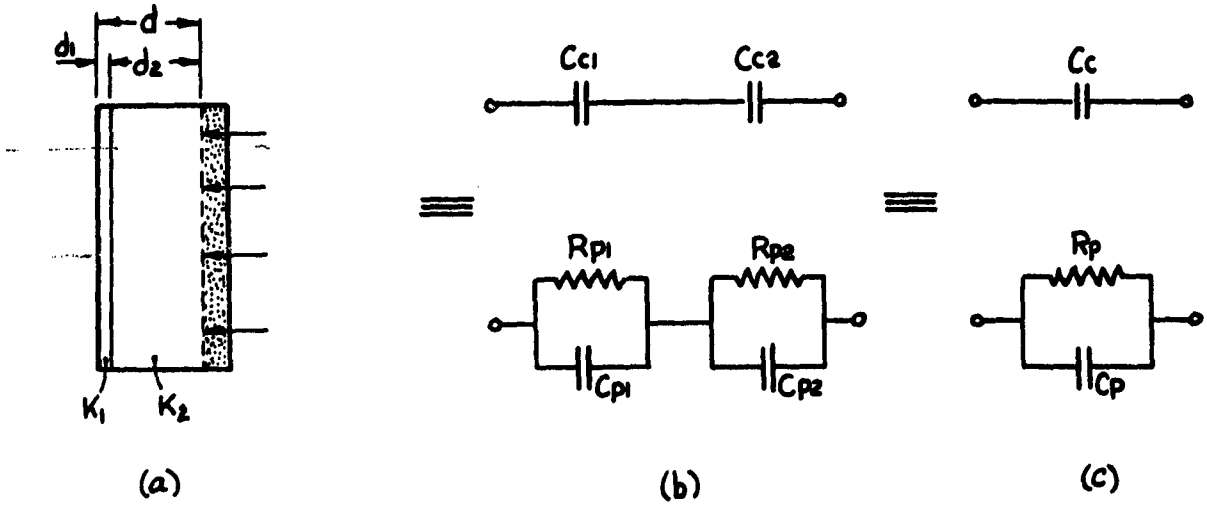

Fig. 3

circuits. Let the complex capacitance of each dielectric be defined respectively by

$$C_{c1} = \frac{A\,\varepsilon_{c1}}{d_1} \quad , \tag{1}$$

$$C_{c2} = \frac{A\,\varepsilon_{c2}}{d_2} \quad , \tag{2}$$

where

A = contact and dielectric area (meters^2),

$\varepsilon_{c1}, \varepsilon_{c2}$ = complex dielectric permittivities (farads/meter),

$\varepsilon_{c1} = \varepsilon_o \left(K_1' - j\,K_1''\right)$ for dielectric K_1,

$\varepsilon_{c2} = \varepsilon_o \left(K_2' - j\,K_2''\right)$ for dielectric K_2,

ε_o = permittivity of empty space (farads/meter),

K_1', K_2' = dielectric coefficients,

K_1'', K_2'' = dielectric loss factors, and

d_1, d_2 = dielectric thicknesses (meters).

Each complex capacitor is viewed to be equivalent to an ideal capacitor C_{p1} and C_{p2} in parallel with a resistor R_{p1} and R_{p2} which incorporates all dissipative losses of the system. The complex admittance Y of each combination is

$$Y_1 = \frac{1}{R_{p1}} + j\omega C_{p1} = j\omega C_{c1} \quad , \text{ and} \tag{3}$$

$$Y_2 = \frac{1}{R_{p2}} + j\omega C_{p2} = j\omega C_{c2} \quad , \tag{4}$$

from which it follows that

$$C_{p1} = \frac{\varepsilon_o K_1' A}{d_1} \quad ; \quad R_{p1} = \frac{d_1}{\varepsilon_o K_1'' \omega A} \quad ; \text{ and} \tag{5}$$

$$C_{p2} = \frac{\varepsilon_o K_2' A}{d_2} \quad ; \quad R_{p2} = \frac{d_2}{\varepsilon_o K_2'' \omega A} \quad . \tag{6}$$

Since dissipation factor D is defined by K''/K', then from (5) and (6)

$$D_1 = \frac{K_1''}{K_1'} = \frac{1}{\omega C_{p1} R_{p1}} = \tan \delta_1 \quad ,$$

$$D_2 = \frac{K_2''}{K_2'} = \frac{1}{\omega C_{p2} R_{p2}} = \tan \delta_2 \quad .$$

Finally, each complex capacitor can be lumped together into one equivalent complex capacitor C_c (Fig. 3c), viz.

$$C_c = \frac{C_{c1} C_{c2}}{C_{c1} + C_{c2}} = \frac{\varepsilon_o A K_1' K_2' (1 - jD_1)(1 - jD_2)}{K_1' d_2 (1 - jD_1) + K_2' d_1 (1 - jD_2)} \quad , \tag{7}$$

which is equivalent to a capacitor C_p paralleled with a resistor R_p *viz.*

$$C_p = \frac{A\varepsilon_o K_1' K_2' [K_1' d_2 (D_1^2+1) + K_2' d_1 (D_2^2+1)]}{K_1'^2 d_2^2 (D_1^2+1) + 2K_1' d_2 K_2' d_1 (D_1 D_2 + 1) + K_2'^2 d_1^2 (D_2^2+1)} \text{ , and} \quad (8)$$

$$R_p = \frac{K_1'^2 d_2^2 (D_1^2+1) + 2K_1' d_2 K_2' d_1 (D_1 D_2 + 1) + K_2'^2 d_1^2 (D_2^2+1)}{\omega A \varepsilon_o K_1' K_2' [K_1' d_2 D_2 (D_1^2+1) + K_2' d_1 D_1 (D_2^2+1)]} \quad (9)$$

The effective dissipation factor for this combination is defined as

$$D_{eff} = \frac{K''_{eff}}{K'_{eff}} = \frac{1}{\omega C_p R_p} = \tan \delta_{eff} \quad (10)$$

where the effective dielectric coefficient is

$$K'_{eff} = \frac{K_1' K_2' [K_1' d_2 (D_1^2+1) + K_2' d_1 (D_2^2+1)][d_1 + d_2]}{K_1'^2 d_2^2 (D_1^2+1) + 2K_1' K_2' d_1 d_2 (D_1 D_2 + 1) K_2'^2 d_1^2 (D_2^2+1)} = \frac{C_p d}{A \varepsilon_o} \text{ , } \quad (11)$$

and the effective dielectric loss factor is

$$K''_{eff} = \frac{K_1' K_2' [K_1' d_2 D_2 (D_1^2+1) + K_2' d_1 D_1 (D_2^2+1)][d_1 + d_2]}{K_1'^2 d_2^2 (D_1^2+1) + 2K_1' K_2' d_1 d_2 (D_1 D_2 + 1) + K_2'^2 d_1^2 (D_2^2+1)} = \frac{d}{\varepsilon_o R_p \omega A} \text{ . } \quad (12)$$

Thus

$$D_{eff} = \frac{K_1' d_2 D_2 (D_1^2+1) + K_2' d_1 D_1 (D_2^2+1)}{K_1' d_2 (D_1^2+1) + K_2' d_1 (D_2^2+1)} \text{ . } \quad (13)$$

EXPECTATION PERFORMANCE

The above analysis is sufficiently general that the relations derived are valid for all parallel plate capacitors with duo-dielectric media (excluding fringing effects). For the device of Fig. 3a, which is currently being fabricated with a frequency invariant silicone dielectric K_1' without losses ($D_1 \cong 0$) to allow better interpretation of photocapacitor behavior, the expectation capacitance ratio between saturated light ($d_2 = 0$) and dark conditions (assuming K_2' is independent of light intensity) is

$$\frac{C_{P_{LIGHT}}}{C_{P_{DARK}}} = \frac{K_1'^2 d_2^2 + 2K_1'K_2' d_1 d_2 + K_2'^2 d_1^2 (D_{2d}^2 + 1)}{K_2' d_1 [K_1' d_2 + K_2' d_1 (D_{2d}^2 + 1)]} \quad , \qquad (14)$$

with an effective dissipation factor change of

$$D_{eff.\,dark} - D_{eff.\,light} = \frac{K_1' d_2 D_{2d}}{K_1' d_2 + K_2' d_1 (D_{2d}^2 + 1)} \quad , \qquad (15)$$

where D_{2d} = dissipation factor of the CdS dielectric in the dark. Since high resistivity CdS material is to be used for the photocapacitor, it is anticipated that $D_{2d} \ll 1$. Therefore

$$\frac{C_{P_{LIGHT}}}{C_{P_{DARK}}} = 1 + \frac{K_1' d_2}{K_2' d_1} \quad . \qquad (16)$$

The capacitance ratio between light and dark will thus be determined only by the duo-dielectric coefficients and their thicknesses. For the device being fabricated $K_1' = 3$, $K_2' = 8$, $d_1 = 0.00035$ inches, and $d_2 = 0.0233$ inches. The total change expected will be about 25 times.

Enormous capacitance changes can be expected when a depletion layer is utilized instead of the silicone dielectric. In this case $K_1' \cong K_2' = 8$, and $d_2/d_1 \cong 1000$, so that changes of 1000 are possible.

PLANS FOR NEXT INTERVAL

Experimental data will be taken on the photocapacitor currently being fabricated and compared with expectation values. Any deviations from expectation values will be examined and studied relative to the assumptions made in deriving (16). The two assumptions most suspect at this time are (a) the CdS dielectric coefficient K_2' is invariant with light intensity and (b) the dissipation factor D_{2d} is negligible. Finally, if this photocapacitor is found to be frequency dependent as implied in earlier more complex units (2nd quarterly report), then it will be necessary to bring in such dependence by introducing dielectric polarization effects or dissipation effects, or both. This is not difficult because of the general approach made in the analysis.

The following papers and texts were found useful in deriving the concepts outlined in this appendix.

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